Distributed Power Delivery for Energy Efficient and Low Power Systems

Selçuk Köse
Department of Electrical Engineering
University of South Florida
Tampa, Florida 33620
kose@usf.edu

Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester
Rochester, New York 14627
friedman@ece.rochester.edu

***Abstract*—With the introduction of ultra-small on-chip voltage regulators, novel design methodologies are needed to determine the location of these on-chip power supplies and decoupling capacitors. In this paper, the optimal location of the power supplies and decoupling capacitors is determined for different size and number of components. Facility location problems are applied to determine the optimum location of power supplies and decoupling capacitors in the proposed methodology.**

I. Introduction

Power consumption has become one of the primary design bottlenecks with the proliferation of mobile devices as well as server farms where the performance per watt is the primary benchmark [1], [2]. The power generated and regulated by the off-chip and on-chip voltage regulators is distributed to billions of load circuits throughout a power distribution system. Due to the parasitic impedances of the power distribution networks, voltage fluctuations in the supply voltage occur. These fluctuations depend on the characteristics of the load current demand and the behavior of the power distribution network. The power supplies are also supported by locally distributed decoupling capacitors which serve as a reservoir of charge to provide current to the load circuits [3]. The complexity of the high performance power delivery systems has increased significantly with the integration of diverse technologies on a single die, forming an heterogeneous system. The required supply voltage levels and the noise constraints vary significantly for different technologies. Novel voltage regulator topologies [4]–[10] have recently been proposed, enabling not only on-chip power supply integration but also multiple on-chip point-of-load power supplies [10]–[12]. These on-chip point-of-load power supplies provide the required voltage close to the load circuits, greatly reducing the effective impedance between the load circuits and power supplies [13].

Next generation power delivery networks for heterogeneous circuits will contain tens to hundreds of on-chip power supplies supported by thousands of on-chip decoupling capacitors to satisfy the current demand of billions of load circuits. The design of these complex systems would be enhanced if available resources such as the physical area, number of metal layers, and power budget were not severely limited. The continuous demand over the past decade for greater functionality within a small form factor has imposed tight resource constraints while achieving aggressive performance and noise targets [14].

Several techniques have been proposed for efficient power delivery systems, typically focusing on optimizing the power network [14], [15] and the placement of the decoupling capacitor [16], [17]. Recently, Zeng *et al.* [18] proposed an optimization technique for designing power networks with multiple on-chip voltage regulators. The design tradeoffs of on-chip voltage regulators and the effect of these regulators on high frequency voltage fluctuations and mid-frequency resonance have been analyzed. The interactions between the power supplies and the decoupling capacitors are, however, not considered, which can significantly affect the performance of an integrated circuit [18]. These interactions are quite critical in producing a robust power distribution network [10]. Decoupling capacitors and on-chip power supplies exhibit several distinct characteristics such as the response time, area requirements, and parasitic output impedance. Circuit models for these components should accurately capture these characteristics while being sufficiently simple to not overly complicate the optimization process.

In this paper, facility location optimization algorithms will be analyzed to determine the optimum location of power supplies and decoupling capacitors to minimize power noise [19]–[21]. The constraints of this power network co-design problem depend on the application and specifications of the performance objectives. The optimization goal can be to minimize the maximum voltage drop, average voltage drop, total area, response time for particular circuit blocks, or total power consumption. Multiple optimization goals can also be applied for smaller or mid-size integrated circuits.

The rest of the paper is organized as follows. A recently developed point-of-load voltage regulator is briefly described in Section II. The facility location problem is introduced with some exemplary applications in Section III. A proposed methodology to determine the optimum location of the power supplies and decoupling capacitors is described in Section IV. The optimum location of the power supplies and decoupling capacitors, determined for a sample circuit, is presented in

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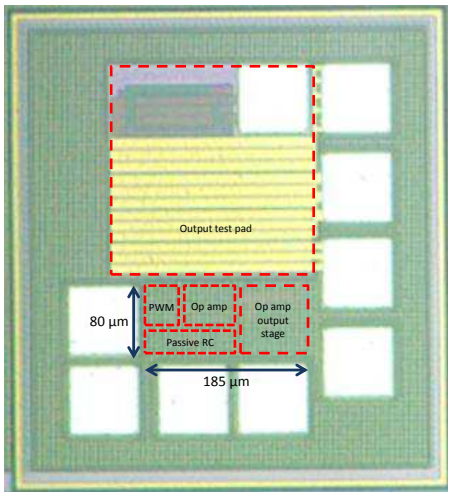


Fig. 1. Microphotograph of the hybrid voltage regulator [8].

Section V. The paper is concluded in Section VI.

II. Point-of-Load Voltage Regulators

Placing multiple point-of-load power supplies is challenging since the area occupied by a single power supply should be small and the efficiency sufficiently high. Guo *et al.* proposed an output capacitorless low-dropout regulator which occupies 0.019 mm^2 on-chip area [6]. The authors also recently proposed a hybrid point-of-load voltage regulator, occupying 0.015 mm^2 on-chip area [8]. A microphotograph of this hybrid point-of-load regulator is shown in Fig. 1. These area efficient voltage regulators provides a means for distributing multiple local power supplies across an integrated circuit, while maintaining high current efficiency and small area. With the proposed voltage regulator, on-chip signal and power integrity is significantly enhanced while providing the capability for distributing multiple power supplies. Design methodologies are therefore required to determine the location, size, and number of these power supplies and decoupling capacitors.

III. Facility Location Problem

Every complex system is composed of small components, typically with simple structures. The interactions and aggregation of these components form a highly complex system. The efficiency of this system strongly depends upon the physical location of these components, which significantly affects the interactions. In most systems, these components can be grouped into two categories; (1) facilities, and (2) customers. The location, size, and number of facilities that minimize the cost of providing a high quality service to the customers are the design objectives [19].

Mathematical models of the location have been used to determine the optimal number, location, and size of the facilities as well as allocate facility resources to the customers that minimize or maximize the objective function [19]–[21]. The problem can be categorized depending upon the network (discrete or continuous) and the input (static or dynamic). The objective is to minimize the average (or maximum) distance from the facilities to the customers, determine the minimum number of facilities that serve a particular number of customers at fixed locations, or maximize the minimum distance from a facility to the customers.

The design of on-chip power delivery networks for heterogeneous circuits exhibits significant similarities to the design of electrical distribution networks in larger scale systems, such as the electric power distribution grid of a city. The electricity generated at a power plant is downconverted and distributed to substation transformers, typically outside a city. The output voltage of these substation transformers is further downconverted and regulated by the local power supplies. This voltage can be either delivered to industrial customers at a high voltage level or further downconverted and regulated at smaller substations and distributed to the local city power grid. Large capacitors are integrated within this electrical distribution system to reduce voltage fluctuations. Alternatively, in an heterogeneous integrated circuit, the on-board voltage regulators downconvert the output voltage of the board level power supply unit. This voltage is delivered to the on-chip voltage regulators or directly to the on-chip power grid which provides current to the load circuits. The required voltage levels and noise constraints are technology and design dependent. The on-chip power delivery system is designed to deliver different voltage levels within noise constraints. Decoupling capacitors are distributed throughout the on-chip power delivery network to support the power distribution system. A parallel can be drawn between the transformers and off-chip voltage regulators, the small substations and on-chip voltage regulators, and the large capacitors and on-chip decoupling capacitors. Additionally, the voltage requirements of different technologies within an heterogeneous integrated circuit vary in a similar manner as the voltage requirements of industrial and residential regions within a city.

Several optimization algorithms have been proposed which consider possible constraints to provide an optimal solution to this problem. Due to the similarity between the electrical distribution network of a city and the power distribution network of a heterogeneous circuit, analogous algorithms can be applied to the design of these systems. Since facility location algorithms are widely used to design electrical distribution networks, these city planning algorithms are leveraged in designing on-chip power networks within heterogeneous circuits.

IV. Proposed Optimization Methodology

These existing optimization techniques and methodologies provide a near optimal solution for the location of the on-chip power supplies and decoupling capacitors that minimize the average (or maximum) power noise. The focus of this paper is to determine the optimal number and location of the on-chip power supplies and decoupling capacitors that minimize the average power noise. A closed-form model of the impedance, proposed in [13], is utilized to determine the effective resistance from the power supplies and decoupling

capacitors to the load circuits. The constraints of the problem are as follows,

- The total area of the power supplies and decoupling capacitors is maintained constant
- All power supplies must be larger than the minimum sized power supply
- All decoupling capacitors must be larger than the minimum sized decoupling capacitor

The proposed objective function is

$$Minimize$$

$$\begin{aligned} F(n,m,k) = K_1 \sum_{j=1}^{m}\sum_{i=1}^{n} C_{P_{ij}}(R_{out}(P_i) + R_{eff}(P_i, L_j)) \\ + K_2 \sum_{j=1}^{m}\sum_{i=1}^{k} C_{D_{ij}}(R_{esr}(D_i) + R_{eff}(D_i, L_j)) \\ + K_3 \sum_{j=1}^{m}\sum_{i=1}^{k} cap_{D_i} N_{tr_{L_j}}(R_{esr}(D_i) + R_{eff}(D_i, L_j)), \end{aligned} \tag{1}$$

$$Subject\ to$$

$$\begin{aligned} &R_{eff}(node_\alpha, node_\beta)/r = \\ &\frac{\sqrt{1}}{2\pi}[ln((x_1 - x_2)^2 + (y_1 - y_2)^2) + 3.44388] - 0.033425, \end{aligned} \tag{2}$$

$$1 < x_{\alpha,\beta} < (Grid\ size)_X, \tag{3}$$

$$1 < y_{\alpha,\beta} < (Grid\ size)_Y, \tag{4}$$

$$C_{P_{ij}} = \frac{G_{ij}}{\sum_{i=1}^{n} G_{ij}}, \tag{5}$$

$$C_{D_{ij}} = \frac{G_{ij}}{\sum_{i=1}^{k} G_{ij}}, \tag{6}$$

$$\sum_{j=1}^{m} C_{P_{ij}} \leq cap_{P_i}, \tag{7}$$

$$\sum_{j=1}^{m} C_{D_{ij}} \leq cap_{D_i}, \tag{8}$$

$$\sum_{i=1}^{n} C_{P_{ij}} + \sum_{i=1}^{k} C_{D_{ij}} = \sum_{i=1}^{m} I_i, \tag{9}$$

$$\sum_{i=1}^{n} cap_{P_i} + \sum_{i=1}^{k} cap_{D_i} \geq \sum_{i=1}^{m} I_i, \tag{10}$$

where the definition of the aforementioned parameters are listed in Table I.

In heterogeneous systems, where the slew rate, operating frequency, and supply voltage vary significantly over different portions of a circuit, K_i provides the flexibility to optimize the power distribution system for different technologies.

TABLE I
DEFINITION OF THE PARAMETERS IN (1)-(10).

Parameter	Definition
P_i	i^{th} power supply
D_i	i^{th} decoupling capacitor
L_i	i^{th} circuit block
$R_{eff}(node_1, node_2)$	Effective resistance between $node_1$ and $node_2$
(x_1, y_1)	Coordinates of $node_1$
(x_2, y_2)	Coordinates of $node_2$
r	Unit resistance within the power grid
n	Number of power supplies
k	Number of decoupling capacitors
m	Number of load circuits
$R_{out}(P_i)$	Output resistance of i^{th} power supply
$R_{esr}(D_i)$	Effective series resistance of i^{th} decap
G_{ij}	Equivalent conductance
K_i	Weighting parameter
$C_{P_{ij}}$	Contribution of i^{th} power supply to j^{th} load
$C_{D_{ij}}$	Contribution of i^{th} decap to j^{th} load
cap_{P_i}	Capacity of i^{th} power supply
cap_{D_i}	Capacity of i^{th} decap
$N_{tr_{L_j}}$	Normalized transition time of the j^{th} load circuit
I_i	Current demand of i_{th} load
$(Grid\ size)_X$	Power grid size in horizontal direction
$(Grid\ size)_Y$	Power grid size in vertical direction

V. CASE STUDY

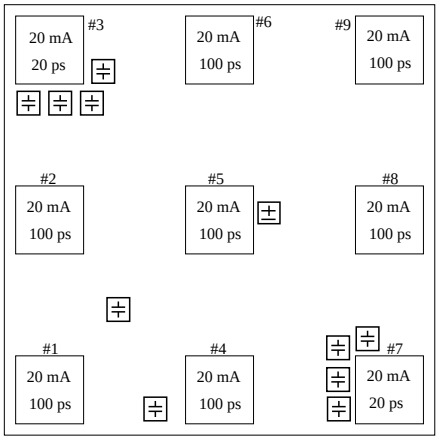
The voltage drop maps of the related circuits with the decoupling capacitors and power supplies located at the predetermined locations are obtained using SPICE. The node voltages, which are determined by the SPICE simulations, are produced from MATLAB.

The optimum number and location of the power supplies and decoupling capacitors that minimize the voltage drop and response time within certain blocks are determined for a small sample circuit, as shown in Fig. 2, to provide an intuitive understanding of the proposed methodology. The sample circuit is composed of nine circuit blocks with different current profiles. The third and seventh blocks have current profiles with a faster transition time (*i.e.*, 20 ps) than the rest of the circuits which have a relatively slower transition time (*i.e.*, 100 ps). Since the decoupling capacitors provide immediate charge, intuitively, the decoupling capacitors should be placed close to those blocks with a fast transition time to provide a fast response to transient changes in the current. The optimum location of the power supplies and decoupling capacitors that minimizes both the maximum voltage drop and response time for certain blocks (the third and seventh blocks) is used, where K_1, K_2, and K_3 are set to one. The optimum location of one large on-chip power supply and ten decoupling capacitors (case a) is shown in Fig. 2a. The power supply is located at a central location to reduce the maximum physical distance to each of the circuit blocks. The decoupling capacitors, however, are placed physically close to the third and seventh blocks. Most of the current demand of these blocks is provided by the surrounding decoupling capacitors. The optimum location of the four relatively low current power supplies and 20 small

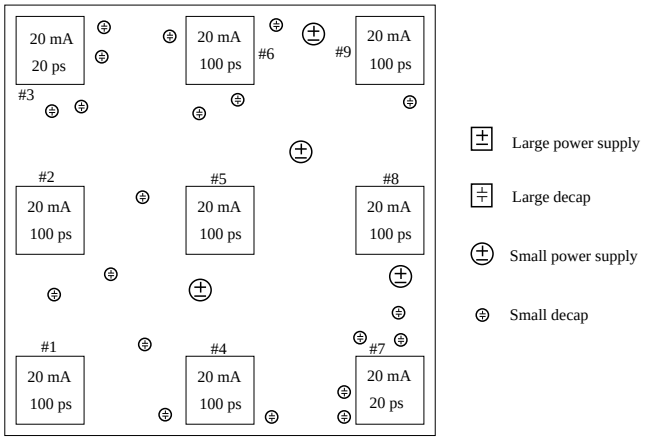
decoupling capacitors (case b) is also determined, as shown in Fig. 2b. In this case, the third and seventh circuit blocks are surrounded by local decoupling capacitors whereas the power supplies are distributed to ensure that the maximum distance from the power supplies to the remaining blocks is minimized. The voltage drop map for these two cases is shown in Fig. 3, where increasing the number of power supplies and decoupling capacitors significantly reduces the voltage drop. The maximum voltage drop is 133 mV and 77 mV, respectively, for cases a and b. More than a 40% reduction in the maximum voltage drop is achieved by increasing the number and distributing the location of the power supplies and decoupling capacitors.

The area of an on-chip power supply is typically dominated by the output pass transistors [22], where the size of these pass transistors changes linearly with the maximum output current demand. The size of an on-chip power supply therefore changes linearly with the maximum output current capacity. Additionally, when the on-chip power supplies are sufficiently small, the ultra-small power supplies are combined to form a larger power supply with a higher output current. In this paper, the size of a power supply is assumed to change linearly with the maximum output current capacity.

The general algebraic modeling system (GAMS) is used as the optimization tool [23]. The proposed optimization methodology is modeled as a mixed integer nonlinear programming problem. The location of the power supplies and decoupling capacitors that minimizes the objective function is determined for different number of power supplies and decoupling capacitors. The total area of the power supplies and decoupling capacitors is maintained the same for all of the test cases to provide a fair comparison.



(a)



(b)

Fig. 2. Floorplan of the example circuit with two different power delivery networks, a) one large power supply with ten decoupling capacitors, and b) four relatively smaller distributed power supplies with 20 small decoupling capacitors.

VI. Conclusions

The similarity between the facility location problem and the design of heterogeneous integrated circuits is exploited. An objective function based on the effective resistance between the power supplies, decoupling capacitors, and load circuits is proposed that minimizes the average voltage drop throughout a heterogeneous integrated circuit. This objective function considers the contribution of current from different power supplies and decoupling capacitors to a circuit block as well as the size of the individual circuit blocks. The optimal location of the on-chip power supplies and decoupling capacitors is determined for a sample circuit.

References

[1] D. Meisner *et al.*, "Power Management of Online Data-Intensive Services," *Proceedings of the ACM International Symposium on Computer Architecture*, pp. 319–330, June 2011.

[2] R. Jakushokas, M. Popovich, A. V. Mezhiba, S. Kose, and E. G. Friedman, *Power Distribution Networks with On-Chip Decoupling Capacitors, Second Edition*, Springer, 2011.

[3] M. Popovich, M. Sotman, A. Kolodny, and E. G. Friedman, "Effective Radii of On-Chip Decoupling Capacitors," *IEEE Transactions on Very Large Scale Integration (VLSI) Circuits*, Vol. 16, No. 7, pp. 894–907, July 2008.

[4] K. N. Leung and P. K. T. Mok, "A Capacitor-Free CMOS Low-Dropout Regulator with Damping-Factor-Control Frequency Compensation," *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 10, pp. 1691–1702, October 2003.

[5] P. Hazucha *et al.*, "Area-Efficient Linear Regulator with Ultra-Fast Load Regulation," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 4, pp. 933–940, April 2005.

[6] J. Guo and K. N. Leung, "A 6-μW Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, Vol. 45, No. 9, pp. 1896–1905, September 2010.

[7] Y. Ramadass, A. Fayed, B. Haroun, and A. Chandrakasan, "A 0.16mm^2 Completely On-Chip Switched-Capacitor DC-DC Converter Using Digital Capacitance Modulation for LDO Replacement in 45nm CMOS," *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 208–209, February 2010.

[8] S. Kose and E. G Friedman, "An Area Efficient Fully Monolithic Hybrid Voltage Regulator," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2718–2721, May/June 2010.

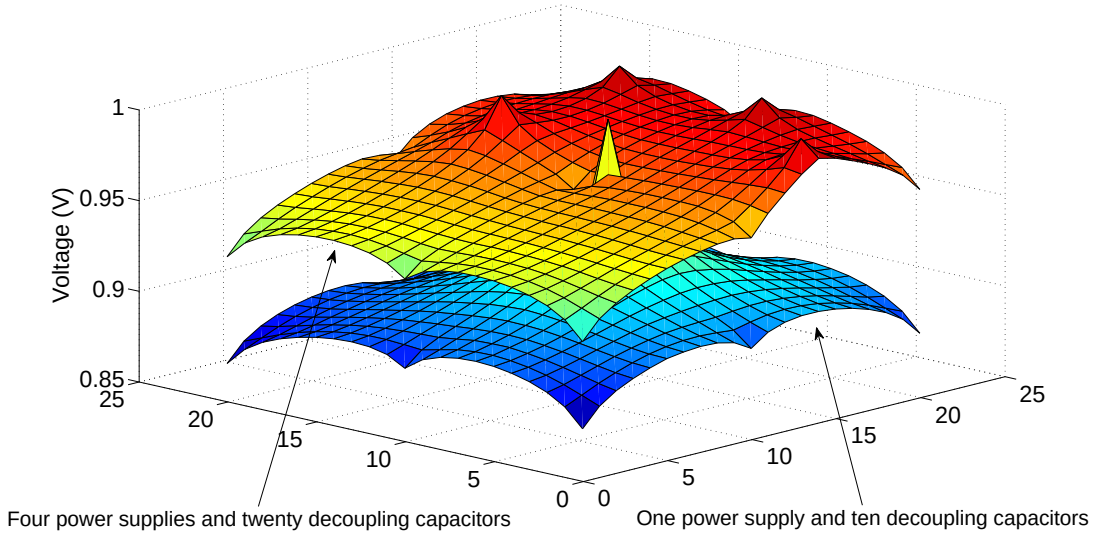


Fig. 3. Map of voltage drops within the sample circuit for two different cases, one large power supply with ten decoupling capacitors, and two relatively smaller distributed power supplies with 20 small decoupling capacitors. The maximum voltage drop is reduced when the number of power supplies and decoupling capacitors is increased due to the distributed nature of the power delivery network.

[9] S. Kose and E. G Friedman, "On-Chip Point-of-Load Voltage Regulator for Distributed Power Supplies," *Proceedings of the ACM Great Lakes Symposium on VLSI*, pp. 377–380, May 2010.

[10] S. Kose and E. G Friedman, "Distributed Power Network Co-Design with On-Chip Power Supplies and Decoupling Capacitors," *Proceedings of the Workshop on System Level Interconnect Prediction*, June 2011.

[11] S. Kose and E. G Friedman, "Distributed On-Chip Power Delivery," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, December 2012.

[12] S. Kose and E. G Friedman, "Simultaneous Co-Design of Distributed On-Chip Power Supplies and Decoupling Capacitors," *Proceedings of the IEEE International SOC Conference*, pp. 15–18, September 2010.

[13] S. Kose and E. G Friedman, "Effective Resistance of a Two Layer Mesh," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 58, No. 11, pp. 739–743, November 2011.

[14] K. Wang and M. Marek-Sadowska, "On-Chip Power-Supply Network Optimization using Multigrid-Based Technique," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 24, No. 3, pp. 407–417, March 2005.

[15] X.-D. S. Tan and C.-J. R. Shi, "Fast Power/Ground Network Optimization Based on Equivalent Circuit Modeling," *Proceedings of the IEEE/ACM Design Automation Conference*, pp. 550–554, June 2001.

[16] M. D. Pant, P. Pant, and D. S. Wills, "On-Chip Decoupling Capacitor Optimization Using Architectural Level Prediction," *IEEE Transactions on Very Large Scale Integration (VLSI) Circuits*, Vol. 10, No. 3, pp. 319–326, June 2002.

[17] M. Popovich, E. G. Friedman, R. M. Secareanu, and O. L. Hartin, "Efficient Placement of Distributed On-Chip Decoupling Capacitors in Nanoscale ICs," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 811–816, November 2007.

[18] Z. Zeng, X. Ye, Z. Feng, and P. Li, "Tradeoff Analysis and Optimization of Power Delivery Networks with On-Chip Voltage Regulation," *Proceedings of the IEEE/ACM Design Automation Conference*, pp. 831–836, June 2010.

[19] M. S. Daskin, *Network and Discrete Location: Models, Algorithms, and Applications*, John Wiley and Sons, 1995.

[20] Z. Drezner and H. Hamacher, *Facility Location: Applications and Theory*, Springer, 2002.

[21] R. Z. Farahani, M. S. Seifi, and N. Asgari, "Multiple Criteria Facility Location Problems: A Survey," *Applied Mathematical Modelling*, Vol. 34, No. 7, pp. 1689–1709, October 2010.

[22] S. Kose, S. Tam, S. Pinzon, B. McDermott, and E. G. Friedman, "Active Filter Based Hybrid On-Chip DC-DC Converters for Point-of-Load Voltage Regulation," *IEEE Transactions on Very Large Scale Integration (VLSI) Circuits*, in press.

[23] A. Brooke, D. Kendrick, and A. Meeraus, *GAMS: A User's Guide*, The Scientific Press, 1992.