On-Chip Point-of-Load Voltage Regulator for Distributed Power Supplies

Selçuk Köse and Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester
Rochester, New York, 14627
[kose,friedman]@ece.rochester.edu

ABSTRACT

An ultra-low area, current efficient voltage regulator appropriate for distributed point-of-load voltage regulation in high performance integrated circuits (ICs) is described in this paper. The proposed voltage regulator is a hybrid combination of a switching voltage regulator and a linear voltage regulator. The voltage regulator can supply over 100 mA current while generating 0.9 volts from a 1.2 input voltage. The current efficiency exceeds 99% while the load regulation to a step current ranges between 40 ns and 60 ns. No output capacitor is required to ensure stability. Hence, the required on-chip area is as small as 0.026 mm^2 for the proposed voltage regulator which is approximately four to six times smaller than area efficient low dropout regulators. The proposed circuit therefore provides a means for distributing multiple local power supplies across an integrated circuit, maintaining high current efficiency and small area.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles—*VLSI(very large scale integration)*

General Terms

Design

Keywords

On-chip voltage regulator, power delivery, DC-DC voltage regulation, active filter

1. INTRODUCTION

Delivering robust and reliable power and ground voltages to high performance circuits has become increasingly difficult with each technology generation. On-chip decoupling capacitors are widely used to provide a low impedance over a wide frequency range [1, 2]. The decoupling capacitors, however, can supply a finite amount of charge to the load devices. On-chip voltage regulators are therefore required for noise sensitive circuits to generate and regulate the supply voltage close to the load circuitry. These on-chip voltage regulators provide charge not only to the load circuitry but also to the decoupling capacitor, enhancing the efficiency of the overall circuit. To deliver a high quality supply voltage to each of the logic blocks in an integrated circuit, multiple on-chip power supplies are required. An area efficient and fast voltage regulator circuit is therefore necessary to provide a high quality on-chip power supply.

DC-DC converters are generally used as power supplies in deep submicrometer integrated circuits. Conventional DC-DC converters can be grouped into three main categories, switching, switched capacitor, and linear DC-DC converters [3, 4]. Buck converters, which are step down switching regulators, are widely used due to the high power efficiency. A second order passive inductor-capacitor (LC) low pass filter is used within a buck converter to filter out the high frequency harmonics of the stepped down voltage. Due to the large area requirement of a passive LC filter, buck converters are generally implemented off-chip.

A more area efficient regulator structure is the low dropout (LDO) voltage regulator [5, 6]. These linear voltage regulators utilize a pass transistor connected to the output of an error amplifier. A large output capacitor is required to ensure stability and fast load regulation. These capacitors are generally implemented off-chip due to the large area requirement. Several techniques have been proposed for implementing a fully monolithic LDO. These techniques, however, require additional circuitry, increasing the on-chip area. LDO regulators exhibit fast load regulation as compared to buck converters. The power efficiency, however, is limited to V_{out}/V_{in}.

Switched capacitor DC-DC converters (or charge pumps) utilize non overlapping switches to charge the capacitor to transfer charge from input to output. These voltage converters dissipate a significant amount of power through the resistive switches. Additionally, the feedback circuitry required to maintain a stable output voltage is difficult to implement.

In this paper, a hybrid combination of a switching and linear voltage regulator is proposed for distributed point-of-load voltage regulation. This circuit provides a means for distributing multiple power supplies across an integrated circuit with fast load regulation and small area. The passive

This research is supported in part by the Semiconductor Research Corporation under Contract No. 2004-TJ-1207, the National Science Foundation under Contract No. CCF-0541206, grants from the New York State Office of Science, Technology & Academic Research to the Center for Advanced Technology in Electronic Imaging Systems, and by grants from Intel Corporation, Eastman Kodak Company, and Freescale Semiconductor Corporation.

GLSVLSI'10, May 16–18, 2010, Providence, Rhode Island, USA.

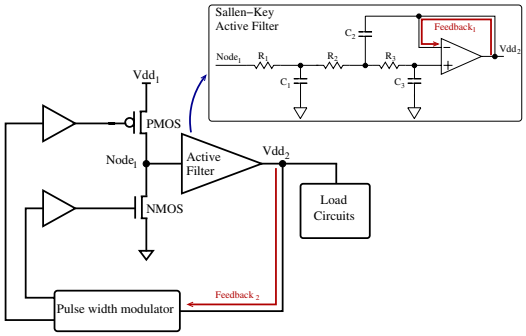

Figure 1: Proposed DC-DC converter. The bulky LC filter is replaced with an active filter and the large tapered buffers are replaced with smaller buffers. Note that two different feedback paths exist which separate the line and load regulation.

LC filter of a buck converter is replaced with an active filter. The idea of replacing the passive filter components with active components was first proposed by Wu *et al.* in [7]. In this paper, however, emphasis is placed on evaluating speed/power/area tradeoffs of several active filter topologies as well as providing feedback circuitry for enhanced stability.

The rest of the paper is organized as follows. The proposed circuit with different active filter topologies and types are discussed in Section 2. Operational amplifier (Op-Amp) design considerations are also discussed in this section. In Section 3, simulation results for several load current demand characteristics are provided for different output voltages. Finally, the paper is concluded in Section 4.

2. ACTIVE FILTER BASED VOLTAGE REGULATOR

To provide a small area on-chip power supply, the passive LC filter in a conventional buck converter is replaced with an active filter structure and the tapered buffers are replaced with smaller buffers, as shown in Fig. 1. Small buffers are sufficient to drive the active filter in the proposed circuit. Replacing the tapered buffers with smaller buffers significantly decreases the power dissipated by the input stage. Alternatively, the output buffers within the Op-Amp dissipate power within the proposed converter. Another characteristic of the proposed regulator is that the feedback required for line and load regulation is satisfied with separate feedback paths, as shown in Fig. 1. Feedback$_1$ is generated by the active filter structure and provides the load regulation whereas feedback$_2$ is optional and can be implemented to control the duty cycle of the switching signal for line regulation. In most cases, feedback$_1$ is sufficient to guarantee fast and accurate load regulation. When only one feedback path is used, the switching signal is generated by simpler circuitry (*e.g.*, a ring oscillator) and the duty cycle of the switching signal is compensated by a local feedback circuit (a duty cycle adjustor). The primary advantage of using a single feedback path is smaller area since feedback$_1$ is provided within the active filter and no additional circuitry is required to implement the compensation structure.

Active filters have been well studied over the last half century [8, 9]. The objective of this section is to review those properties of active filters which affect the design of the proposed voltage regulator while providing relevant background material. Active filter configurations and topologies are reviewed in Section 2.1. In Section 2.2, the design of the Op-Amp is discussed.

2.1 Active Filter Design

Active filter structures have no passive inductors. Alternatively, capacitors, resistors, and an operational amplifier are utilized to implement the filtering function. Certain design considerations should be considered when utilizing an active filter as a voltage regulator since the appropriate active filter topology depends upon the application [9]. For a voltage regulator, the on-chip area requirement, sensitivity of the active filter to component parameter variations (due to aging, temperature, and process variations), and the power dissipated by the active components should be low. Two topologies are popular for implementing an integrated low pass active filter, multiple feedback and Sallen-Key [8]. Multiple feedback low pass filters use capacitive and resistive components within the feedback path from the output to the input node. A DC current path exists between the input and output nodes due to the resistive feedback. The DC current increases the power dissipated by the multiple feedback active filter. Alternatively, Sallen-Key low pass filters only use capacitive feedback. Hence, the static power dissipation of the Sallen-Key topology is significantly less than the multiple feedback topology.

A third order low pass unity-gain Sallen-Key filter topology is shown in Fig. 1. The first section, R_1 and C_1, forms a first order low pass RC filter. R_2, R_3, C_2, C_3, and the Op-Amp form a second order Sallen-Key low pass filter. No DC current path exists between the input and output. Since reducing power dissipation is crucial to the proposed circuit, a unity-gain topology is chosen. The transfer function of the active filter, shown in Fig. 1, is

$$\frac{V_{out}}{V_{in}} = \frac{1}{a_1 s^3 + a_2 s^2 + a_3 s + a_4}, \tag{1}$$

where

$$\begin{aligned} a_1 &= R_1 R_2 R_3 C_1 C_2 C_3, \\ a_2 &= R_1 C_1 C_3 (R_2 + R_3) + R_3 C_2 C_3 (R_1 + R_2), \\ a_3 &= R_1 C_1 + C_3 (R_1 + R_2 + R_3), \\ a_4 &= 1. \end{aligned}$$

A Chebyshev filter type is chosen for the active filter due to the steep roll-off factor as compared to other filter structures which do not require resistive components connected to ground to implement finite zeros. Since a third order Chebyshev filter exhibits no attenuation at DC, the ripple amplitude can be chosen to be high to increase the quality factor Q of the filter, thereby, increasing the slope of the cutoff transition. Larger capacitors in the active filter are required to implement the filter with a larger ripple amplitude. A tradeoff therefore exists between the rolloff factor and the size of the capacitors, C_1, C_2, and C_3. The ripple amplitude is selected to be 1 dB. The value of the parameters a_1, a_2, and a_3 are selected from Chebyshev filter tables [9]. The per cent change in the cutoff frequency and the Q factor of the third order Sallen-Key filter shown in Fig. 1 are listed in Table 1 when the parameter values are individually increased by 1%.

2.2 Op-Amp Design

The performance of an active filter depends upon the performance of the Op-Amp. The gain-bandwidth (GB) prod-

Table 1: Sensitivity analysis for a third order Sallen-Key filter. Per cent change in cutoff frequency and Q factor when individual parameter values are increased by 1%.

	R1	R2	R3	C1	C2	C3
Q	0	-0.4	0.4	0	-0.5	0.5
Cut-off frequency	-1	-0.5	-0.5	-1	-0.5	-0.5

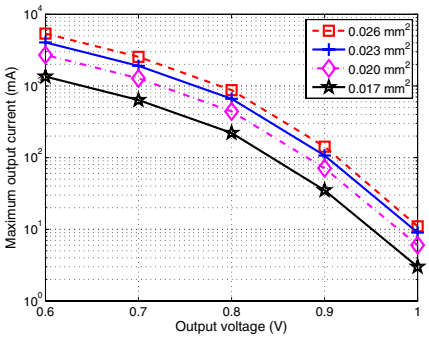

Figure 2: Maximum current delivered to the load circuitry when various output voltages are generated. The maximum current for a particular output voltage can be increased by adding more parallel output stages within the Op-Amp.

uct of the Op-Amp determines the bandwidth of the active filter. Most of the power loss takes place within the Op-Amp structure. The current provided to the output load is supplied by the Op-Amp output stage. Hence, the Op-Amp provides hundreds of milliamps of current to the load devices while maintaining sufficient performance to support reliable active filter operation.

A three stage differential-input single-ended CMOS Op-Amp structure is utilized in the proposed circuit [10]. The first stage is a PMOS differential-input stage, the second stage is a common-source stage, and the third stage is a source follower. The size of the transistors in the third stage is considerably larger than the transistors in the first two stages to supply sufficient current to the load circuitry. The first and second stages are the gain stages which provide a cascade gain of more than 50 dB. The gain of the third stage is close to unity. The overall three stage gain is therefore close to 50 dB with a phase margin of 51°.

3. SIMULATION RESULTS

The proposed active filter based DC-DC voltage converter has been designed in a 90 nm CMOS technology. The input switching signal frequency is 100 MHz. A modified ring oscillator is utilized to supply the switching signal to the input. Since there is no need for large tapered buffers, the power dissipated by the ring oscillator and output buffers is relatively small. The size of the transistors at the output stage of the Op-Amp can be changed for different output voltage or load current demand. The on-chip area of the proposed regulator therefore depends upon the required output voltage and load current characteristics, as illustrated in Fig. 2. A 52% increase in area results in more than a three times increase in the current supplied to the load circuitry. The maximum total on-chip area is less than 0.026 mm^2. Unlike other linear regulators, no capacitor is connected at

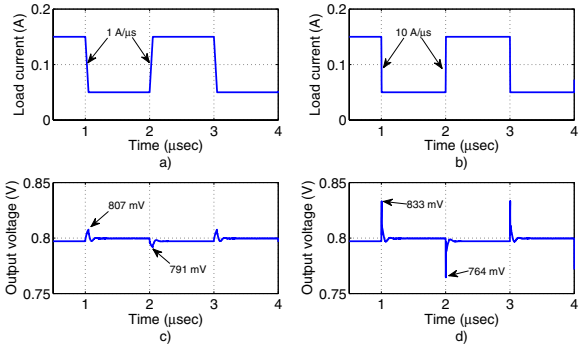

Figure 3: Load regulation of Circuit I. The output current ranges between 50 mA and 150 mA with rise and fall transition slopes of (a) 1 A/μs and (b) 10 A/μs. The output voltage waveforms are shown in (c) for 1 A/μs and (d) for 10 A/μs transition slopes.

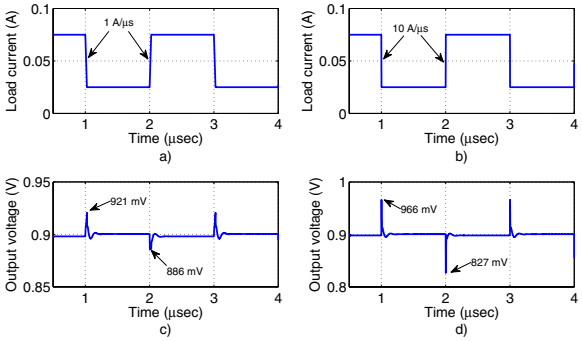

Figure 4: Load regulation of Circuit II. The output current ranges between 25 mA and 75 mA with rise and fall transition slopes of (a) 1 A/μs and (b) 10 A/μs. The output voltage waveforms are shown in (c) for 1 A/μs and (d) for 10 A/μs transition slopes.

the output node, making the proposed circuit convenient for point-of-load voltage regulation.

Two circuits, Circuit I and Circuit II, are described that generate, respectively, 0.8 and 0.9 volts from a 1.2 volt input voltage. The size of the transistors at the output stage of the Op-Amp is larger for the circuit generating 0.9 volts. The area required for Circuit I and Circuit II is 0.017 mm^2 and 0.026 mm^2, respectively. The duty cycle of the input switching signal is 67% and 75% to generate 0.8 and 0.9 volts, respectively. The load regulation is shown in Figs. 3 and 4 for Circuit I and Circuit II, respectively.

The output current is varied from 50 mA to 150 mA and 25 mA to 75 mA with different transition slopes while generating 0.8 and 0.9 volts, respectively. These simulation results are summarized in Table 2. An advantage of the proposed circuit is the output voltage settles at the desired voltage level regardless of the output current demand. That is, the current demand from the load circuitry does not produce a significant DC voltage shift in the output voltage. Additionally, the amplitude of the voltage spikes at the output voltage node is less than 9% of the output voltage despite abrupt changes in the output current demand (*e.g.*, 10 A/μs slope).

The proposed regulator dissipates 0.25 mA quiescent current and can deliver over 220 mA current to the load circuitry while generating 0.8 volts. The quiescent current in-

Table 2: Simulation Results

Output current transition slope		0.8 volts		0.9 volts	
		Fall transition	Rise transition	Fall transition	Rise transition
1 A/μs	Response time (ns)[a]	N/A[b]	40	57	55
	Amplitude of voltage spike (mV)	7	-9	21	-14
	% of voltage spike	0.88%	1.13%	2.33%	1.56%
10 A/μs	Response time (ns)	42	43	47	20
	Amplitude of voltage spike (mV)	33	-36	66	-73
	% of voltage spike	4.13%	4.5%	7.33%	8.11%

[a]Response times are recorded when the amplitude of the voltage spikes is less than 1% of the generated voltage.
[b]Since the amplitude of the voltage spike is already less than 1% of the output voltage, the response time is N/A.

Table 3: Performance of the Proposed Circuit

	[5]	[6]	Circuit I	Circuit II
Year	2005	2007	2009	2009
Technology (nm)	90	350	90	90
V_{in} (V)	1.2	2.0 - 5.5	1.2	1.2
V_{out} (V)	0.9	1.8 - 3.15	0.8	0.9
I_Q (mA)	6	0.02	0.25	0.38
I_{max} (mA)	100	200	220	140
Current eff. (%)	94.3	99.8	99.8	99.5
Response time (ns)	0.54	270	43	57
Chip area (mm^2)	0.098	0.264	0.017	0.026
Output shift (mV)	90	54	8	9

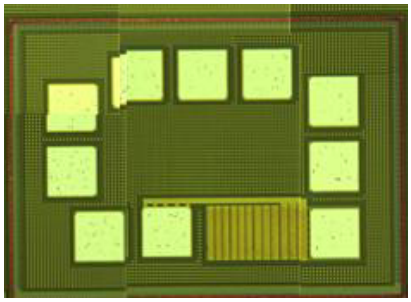

Figure 5: Microphotograph of the active filter-based voltage regulator.

creases to 0.38 mA when the output voltage is 0.9 volts due to the larger output buffer. The current efficiency is greater with increasing current demand. When the output current demand is more than 40 mA, the current efficiency exceeds 99%. A limitation on the maximum output voltage exists due to the NMOS transistors at the output of the Op-Amp. When the output voltage is larger, the effective voltage across N_5 is smaller, limiting the maximum current that N_5 can supply to the load circuitry.

A performance comparison of the proposed circuit with other linear DC-DC converters is listed in Table 3, where [5] and [6] are LDO regulators. Note that the on-chip area required by the proposed circuit is significantly less than the other circuits (about four to six times smaller than an area efficient LDO [5]). Furthermore, the DC shift at the generated voltage is around 1% of the output voltage for different voltage and current requirements, which is significantly smaller as compared to the other example regulator circuits.

Circuit II has been fabricated in an 0.11 um CMOS technology. A microphotograph of the circuit is shown in Fig. 5. The voltage regulator occupies 0.025 mm^2 on-chip area.

4. CONCLUSIONS

A hybrid combination of a switching and linear voltage regulator appropriate for distributed point-of-load voltage regulation is proposed in this paper. The bulky passive LC filter within a buck converter is replaced with an active filter structure to minimize the on-chip area while realizing distributed point-of-load voltage regulation. Design requirements and tradeoffs of both an active filter and an Op-Amp structure are discussed. The area required for the proposed active filter power supply is approximately four to six times smaller than a low area LDO regulator [5]. The amplitude of the voltage spikes at the output is less than 2.5% of the desired output voltage when the output current transitions with a slope of 1 A/μs. When the output current transitions faster (such as 10 A/μs), the amplitude of the voltage spikes is less than 9% of the desired output voltage. The current efficiency is over 99% when the output current demand is greater than 40 mA. The need for an off-chip capacitor or advanced circuit techniques to satisfy stability and performance requirements is eliminated in the proposed circuit. This circuit provides a means for distributing multiple power supplies across an integrated circuit, maintaining high efficiency and small area.

5. REFERENCES

[1] L. Smith *et al.*, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," *IEEE Transactions on Advanced Packaging*, Vol. 22, No. 3, pp. 284–291, August 1999.

[2] M. Popovich, A. V. Mezhiba, and E. G. Friedman, *Power Distribution Networks with On-Chip Decoupling Capacitors*, Springer, 2008.

[3] V. Kursun and E. G. Friedman, *Multi-Voltage CMOS Circuit Design*, New York: Wiley, 2006.

[4] V. Kursun, S. G. Narendra, V. K. De, and E. G. Friedman, "Analysis of Buck Converters for On-Chip Integration with a Dual Supply Voltage Microprocessor," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 11, No. 3, pp. 514–522, June 2003.

[5] P. Hazucha *et al.*, "Area-Efficient Linear Regulator with Ultra-Fast Load Regulation," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 4, pp. 933–940, April 2005.

[6] M. Al-Shyoukh, H. Lee, and R. Perez, "A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator with Buffer Impedance Attenuation," *IEEE Journal of Solid-State Circuits*, Vol. 42, No. 8, pp. 1732–1742, August 2007.

[7] C. H. Wu, L. R. Chang-Chien, and L. Y. Chiou, "Active Filter Based On-Chip Step-Down DC-DC Switching Voltage Regulator," *Proceedings of the IEEE International TENCON Conference*, pp. 1–6, November 2005.

[8] P. R. Sallen and E. L. Key, "A Practical Method for Designing RC Active Filters," *IRE Transactions of Circuit Theory*, Vol. CT-2, pp. 74–85, March 1955.

[9] G. Daryanani, *Principles of Active Network Synthesis and Design*, Wiley, 1976.

[10] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, Wiley, 1997.