Current Profile of a Microcontroller to Determine Electromagnetic Emissions

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***Abstract*—A methodology is proposed to determine the current profile early in the design process to accurately estimate electromagnetic emissions. Design information describing the clock and power distribution network topologies and the placement and sizing of the decoupling capacitors is used to determine the current signatures of individual circuit blocks and the entire system. The proposed methodology is incorporated within the integrated circuit emission model (ICEM). Current profiles for various circuits with different characteristics are determined using the proposed model.**

I. Introduction

Simultaneous switching noise degrades the performance of both the nearby on-chip circuitry which resides on the same die as well as the off-chip circuitry through conducted and radiated electromagnetic emissions [1]. Power and ground distribution networks act as a noise transfer medium. Through this medium, noise propagates to other regions of the circuit and is manifested as fluctuations in the supply voltage. The physical characteristics of the power/ground networks significantly affect the amplitude of these noise fluctuations. This noise propagates from the I/O pads and bonding wires to the off-chip circuits [2]. The wires on the printed circuit board (PCB) can behave as an antenna, generating radiated emissions which can degrade neighboring circuits or appliances [3].

To evaluate the detrimental effects of the noise generated by the switching activity of the circuit blocks, current activity profiles of the switching circuits should be accurately estimated [4], [5]. Traditionally, the current consumption of a circuit block is modeled as a triangular waveform with finite rise/fall transition times, and the total current profile is estimated by overlapping these triangular waveforms. The delay among these circuit blocks due to different clock arrival times is often not considered. Assuming that all of the switching activity occurs simultaneously, the estimated current profile exhibits significantly faster transition times as compared to the actual current activity. The current profile of a circuit block depends upon multiple parameters such as the parasitic impedances and topology of the power/ground and clock distribution network, size and placement of the decoupling capacitors, and parasitic impedances within the package. Moreover, accurate estimation of the current activity using conventional methods and simulation tools is a highly challenging task due to the size and complexity of modern integrated circuits.

Over the last two decades, several techniques have been proposed to characterize the emission level of an integrated circuit by estimating the current profile. Some of these techniques, such as the input/output buffer information specification (IBIS) [6], interface module for integrated circuits (IMIC) [7], integrated circuit emission model (ICEM) [8], and linear equivalent circuit and current source (LECCS) [9] have become international standards by regulatory committees.

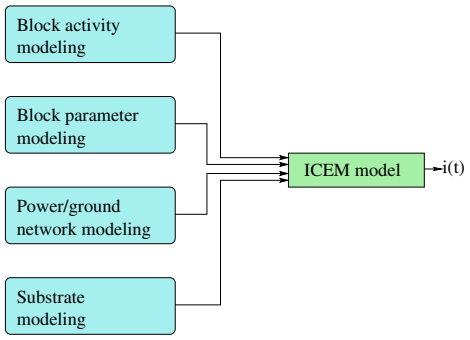

Fig. 1. Conventional ICEM model considering different characteristics of a circuit.

IBIS [6] is a behavioral modeling technique to provide table based buffer information describing the electrical characteristics of the inputs and outputs of a circuit block. Voltages and currents with corresponding timing information of the input/output pins can be estimated with IBIS models. These models do not contain any proprietary data; therefore, the models are provided by semiconductor vendors to evaluate the effect of a particular circuit block on another circuit. IBIS models, however, do not consider any activity internal of the circuits blocks, the primary source of electromagnetic emissions. To overcome these issues with the IBIS model, the IMIC [7] model has been developed to more accurately estimate power/ground noise. The layout information required to generate an IMIC model can include proprietary information. ICEM [8] is a complementary model to IBIS that considers the characteristics of the power/ground network and the switching current activity of the circuit blocks. Voltage fluctuations in the power/ground networks can therefore be estimated more accurately with ICEM. A standard ICEM modeling flow is shown in Fig. 1, where the switching activity, characteristics of the circuit blocks, parasitic impedance and topology of the power/ground network, and substrate models are inputs to ICEM and the output is the current profile of the corresponding circuit blocks.

A current activity modeling methodology is described in this paper for incorporation within the ICEM flow, as shown in

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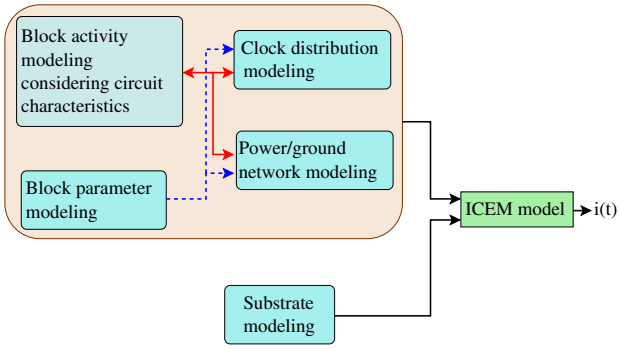

Fig. 2. Proposed current activity modeling methodology that considers the interactions among the current activity profile, clock distribution topology, and parasitic impedances of the power/ground distribution network.

Fig. 2. Interdependencies among the timing characteristics of the switching events, clock distribution topology, and parasitic information describing the power/ground distribution network are included in the proposed methodology.

The rest of the paper is organized as follows. The proposed methodology is described in Section II. Current activity profiles of several circuit blocks with different clock distribution topologies, power/ground parasitic impedances, and sizes are determined with the proposed methodology, which is described in Section III. Finally, the paper is concluded in Section IV.

II. Proposed Methodology

Three design parameters primarily affect the current profile characteristics: the clock distribution network, power distribution network, and digital circuit blocks. The proposed modeling methodology considers the clock distribution network topology, characteristics of the circuit block, and power/ground distribution network topology and parasitic impedances, which is illustrated in the flowchart shown in Fig. 3. The current profile is estimated based on the circuit characteristics and clock topology, and the power/ground noise is determined for the estimated current profile. This power/ground noise is revised considering the size and placement information of the decoupling capacitors. The current profile is updated based on the power/ground noise since this noise significantly affects the current profile. This iterative process continues until the difference between the estimated current profiles in two consecutive steps is less than a predetermined threshold, as shown in Fig. 3.

A. Clock Distribution Network Topology

The clock distribution networks can dramatically affect system-wide performance. Depending upon the system speed, physical area, and power dissipation, different design methodologies and network topologies are possible. The most common and general approaches are tree, H-tree, mesh-tree, and chain [10].

The clock distribution network topology and repeater characteristics [11] are considered in the proposed current activity model. The arrival time of the clock signal to the circuit clusters and the degradation of the transition time of the clock signals are initially determined based on the repeater characteristics, assuming an ideal power/ground distribution network. Degradation of the transition times as compared to a reference clock signal is later modified considering the parasitic impedances of the power grid, as explained in Section II-C.

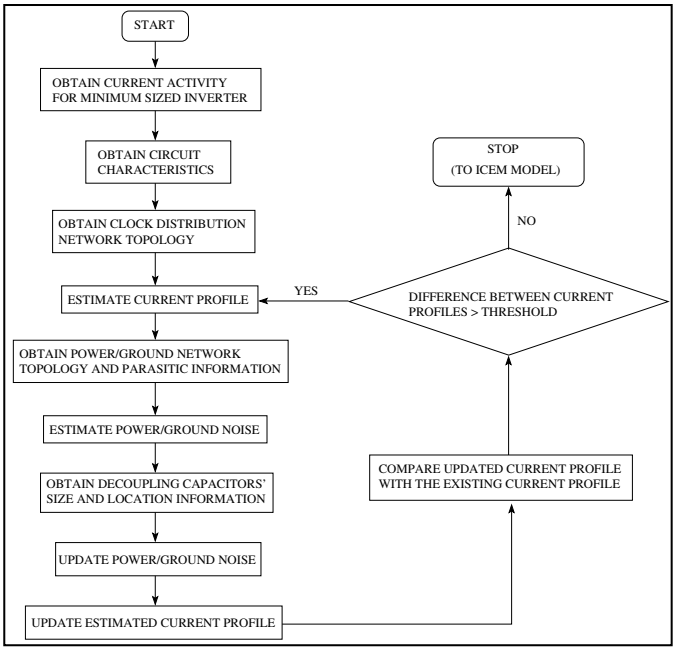

Fig. 3. Flowchart summarizing the proposed methodology integrated within the ICEM flow.

B. Circuit Block Characteristics

A circuit cluster is a group of logic circuits that switch synchronously. The switching activity of a cluster is determined as follows. The number of logic gates within a cluster is determined by dividing the area of the cluster by the area of a minimum sized inverter, as the size of a minimum inverter for a particular technology node is known *a priori*. The number of inverters is multiplied by the activity factor of the block – which is typically between 0.1 and 0.3 – to determine the number of inverters switching during a clock cycle. The current profile of a minimum size inverter is estimated for the technology. The total current profile of a circuit block is the summation of the time shifted current profiles of the individual clusters, where the time shift depends upon the clock network topology.

C. Parasitic Impedance of Power Distribution Topology

A global power distribution network typically provides current to all of the clusters within a circuit. The local power distribution network within a cluster is treated as ideal (*e.g.,* the parasitic impedance of the local power distribution network is negligible). The voltage drop in each cluster within a circuit block is determined separately in the proposed method. Since decoupling capacitors directly influence the voltage drops, the effect of the decoupling capacitors based on the size and placement within the block is also considered.

A decoupling capacitor provides charge to the closest clusters since the local parasitic impedances are less significant [12]. The transition time of the signals within the clusters is also important in determining the effectiveness of a decoupling capacitor. The response time of a decoupling capacitor is determined by the delay of the interconnect between the decoupling capacitor and a particular cluster. When the response time is shorter than the transition times of the signals within the cluster, the capacitor provides charge to that cluster. The amount of charge that can be provided depends upon both the capacitor size and the current required by the switching circuit.

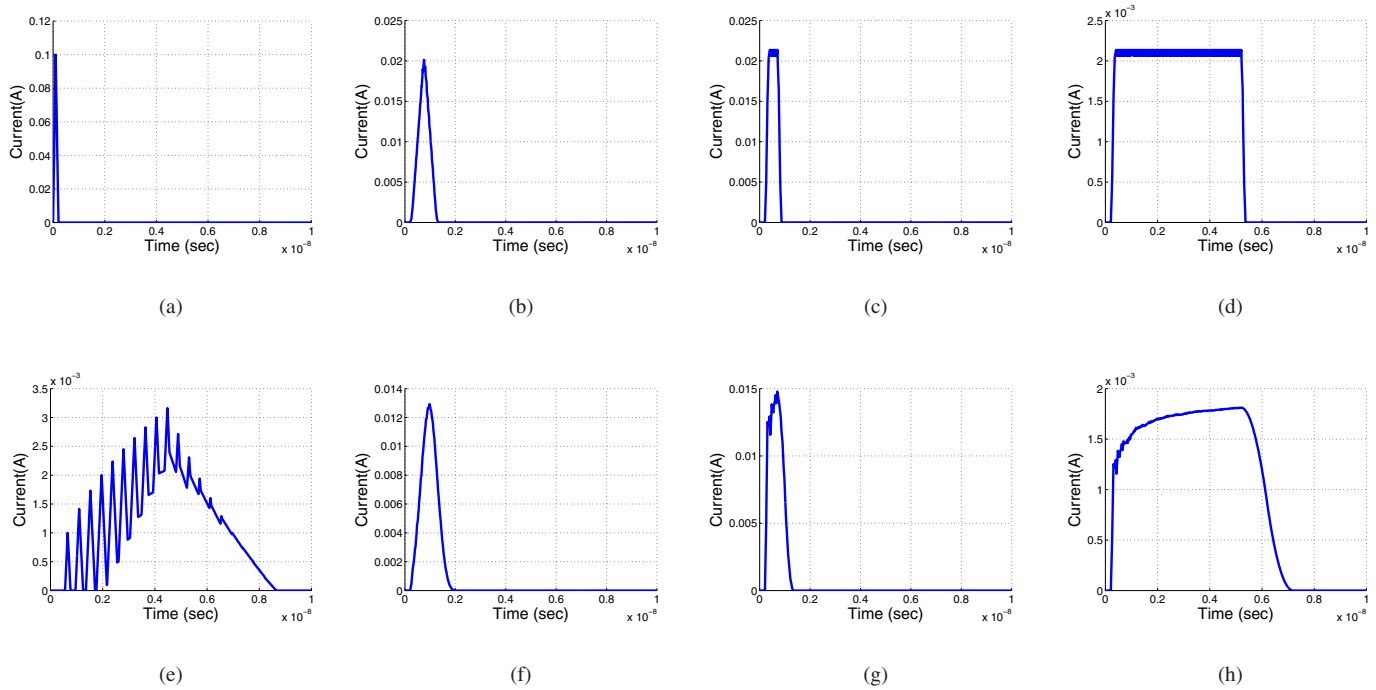

Fig. 4. Current profiles for circuits with various clock and power network characteristics; a) Circuit 1, b) Circuit 2, c) Circuit 3, d) Circuit 4, e) Circuit 5, f) Circuit 6, g) Circuit 7, and h) Circuit 8.

In the proposed method, the parasitic impedance between each decoupling capacitor and the neighboring clusters is determined. The current profile, determined without considering the decoupling capacitors, as discussed in Section II-B, is updated after estimating the effective transition time of the signals within the clusters. The response time of each decoupling capacitor is based on the location and size of the capacitor. The charge provided by a decoupling capacitor to each cluster depends upon the response time of the capacitor and the effective transition time of each adjacent cluster. The decoupling capacitor is assumed to provide no charge to those clusters with a parasitic impedance greater than three times the impedance of the path closest to the cluster. Additional charge is provided to those blocks with less parasitic impedances. This process is performed for each decoupling capacitor.

Once the voltage drop at each cluster is determined, the current profiles of each block are updated by scaling the current with the appropriate *I-V* model. This iterative process of determining the current profiles and voltage drops is repeated until the results converge, as illustrated in Fig. 3.

III. Case Study

Current activity profiles have been determined based on the proposed methodology for eight different circuits, as listed in Table I. The current profile of a circuit exhibits a fast transition time, as shown in Fig. 4a, when the clock signal simultaneously arrives at the circuit clusters. When the number of repeaters within the clock distribution network is limited, the transition time of the clock signal is degraded, as shown in Figs. 4e, 4f, 4g, and 4h. Note that the size of the circuit and clock network have a significant effect on the shape of the current profile. For example, circuits 5 and 7 have the same clock topology and repeater characteristics, but these circuits exhibit different current profiles, as shown in Figs. 4e and 4g, since the size of circuit 5 is greater than the size of circuit 7.

TABLE I
Clock network topology and repeater characteristic of the circuits. Note that certain circuits are larger and the corresponding current profile is different although these circuits have the same clock topology and repeater characteristics.

	Current profile	Clock network	Repeater	Size
Circuit 1	Fig. 4a	H-tree	Yes	100 clusters
Circuit 2	Fig. 4b	Tree	Yes	100 clusters
Circuit 3	Fig. 4c	Mesh	Yes	100 clusters
Circuit 4	Fig. 4d	Chain	Yes	100 clusters
Circuit 5	Fig. 4e	Mesh	No	500 clusters
Circuit 6	Fig. 4f	Tree	No	100 clusters
Circuit 7	Fig. 4g	Mesh	No	100 clusters
Circuit 8	Fig. 4h	Chain	No	100 clusters

An integrated circuit model with 16 clusters has also been developed, as shown in Fig. 5. Each cluster includes an individual mesh structured power distribution network, where the global power distribution network is structured as a power tree, as illustrated in Fig. 5. The current profile of each cluster without considering the global power grid impedances is shown in Fig. 6a. The parasitic impedances of the global power network are included within the model, permitting the voltage drop within the power distribution network to be determined with the proposed approach. The current profile for each cluster is updated by considering the power/ground noise, as illustrated in Fig. 6b.

For example, the voltage drop in cluster 15 is greater than the voltage drop in cluster 3 since cluster 15 is farther from the power supply as compared to cluster 3 (*i.e.*, the parasitic impedance between the power supply and cluster 15 is greater than the parasitic impedances between the power supply and cluster 3). A similar conclusion can be drawn for all of the other blocks. The voltage drop is smallest for cluster 1, whereas the voltage drop is greatest in clusters 14 and 15 due to the largest parasitic impedances.

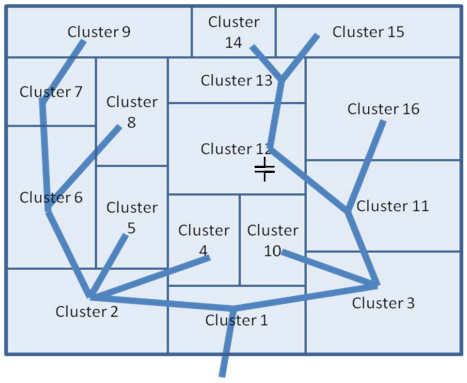

Fig. 5. A circuit with 16 clusters. Each cluster is connected to a global power distribution network which provides current to the local power distribution networks. The power is distributed by a global tree structure and a mesh structure inside the clusters. The power pad is connected from cluster 1 and the power is distributed from block one. Another scenario is that cluster 1 contains a voltage regulator and the power is distributed from that voltage regulator to the entire circuit.

A decoupling capacitor is inserted within cluster 12, where the effect of this capacitor on the power supply noise and current profiles of cluster 12 and the neighboring clusters is investigated. The voltage drop is reduced in cluster 12 and the neighboring clusters. A smaller voltage drop in the supply voltage produces a higher peak current. The current profile of all of the clusters when a decoupling capacitor is inserted within cluster 12 is illustrated in Fig. 6c. The peak current is greater for clusters 12, 13, 14, 15, 11, and 3 due to the close proximity to the decoupling capacitor as compared to the case without the decoupling capacitor. The effect of the decoupling capacitor is most prominent for cluster 12 due to the faster response time of the capacitor. After determining all of the current profiles for each cluster in the circuit by considering both the parasitic impedances of the power network and the decoupling capacitors, the total current profile of the circuit is determined by summing the current profiles of each cluster.

IV. Conclusions

A current profile modeling methodology integrated within a conventional ICEM flow is proposed in this paper. Since the characteristics of the clock distribution network are incorporated within the proposed methodology, the switching activity is more accurately captured by considering the arrival time of the clock signal. The effect of the decoupling capacitors on reducing power/ground noise is also considered in this methodology. The size and location of the capacitors determine the current contribution from the capacitor to the adjacent clusters. The proposed methodology therefore provides enhanced insight into estimating the radiated and conducted emissions caused by on-chip switching activity.

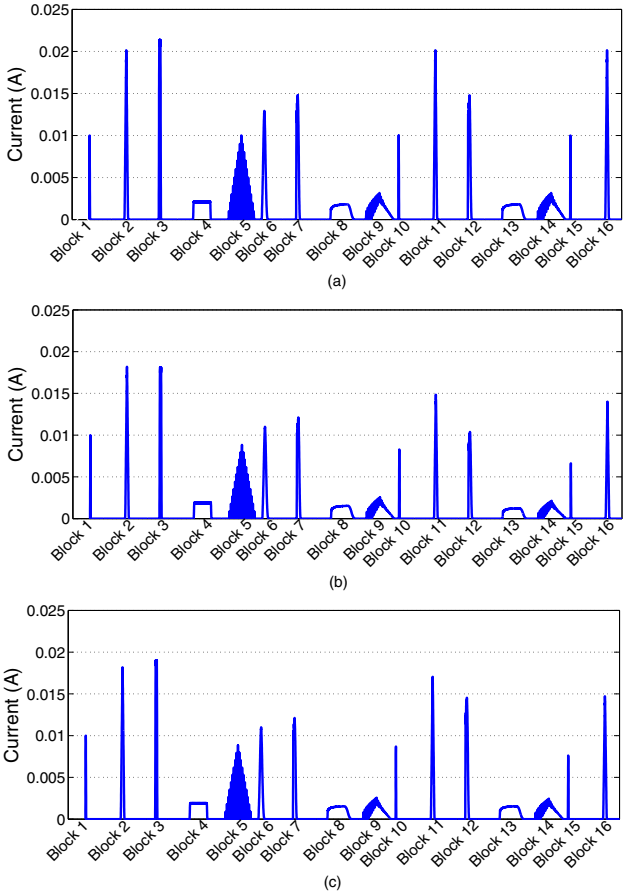

Fig. 6. Current profile of individual circuit clusters shown in Fig. 5 when a) the parasitic impedance of the power network is neglected, b) the parasitic impedance of the power network is considered, and c) a decoupling capacitor is inserted within cluster 12 and the parasitic impedances of the power network are considered.

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