An Enhanced Pulse Width Modulator with Adaptive Duty Cycle and Frequency Control

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***Abstract*- A digitally controlled pulse width modulator (PWM), targeting on-chip power management applications is proposed in this paper. A current starved ring oscillator, with digitally controlled current source based headers and footers, is used to provide a versatile duty cycle and an accurate frequency control. The proposed circuit achieves i) a controlled duty cycle that can vary between 20% and 90% and ii) a compensation circuit that guarantees a constant duty cycle under process, voltage, and temperature (PVT) variations. A fast response time of 5 ns – 20 ns with a fine duty cycle granularity has been achieved through the proposed control techniques. The circuit operates at a frequency range of 500 MHz – 1.66 GHz and is implemented with a 22 nm CMOS predictive technology model.**

I. INTRODUCTION

A pulse width modulator (PWM) is used to generate a periodic switching signal with a varying duty cycle and can be configured to control the duty of a switching signal. Various architectures have been proposed to generate pulse width modulated signals. A voltage controlled oscillator, a counter, a digital to analog converter, and a comparator are used as the building blocks of a PWM [1]. This counter based PWM requires additional clock and reference signals and therefore suffers from large power consumption. PWMs based on either a delay line multiplexor and a ring oscillator multiplexor are described, respectively, in [2] and [3] which consume less power but occupy a large chip area due to the large multiplexor circuits. PWMs based on a delay line multiplexor and a ring oscillator counter provides a means to control area/power tradeoffs [4]. A small and power efficient on-chip PWM requires a small and power efficient oscillator. A modified ring oscillator circuit is proposed to satisfy these requirements within the PWM.

A conventional ring oscillator circuit is shown in Fig. 1. Duty cycle and frequency control are achieved by controlling the supply current of individual inverter stages [5]-[6]. Changing the supply current of individual inverter stages within a ring oscillator affects the transition delay characteristics of the corresponding stages, resulting in an output with a variable duty cycle. PVT variations affect the delay characteristics of the stages resulting in duty cycle variations. Several methods have been proposed to compensate the effects of PVT variations on the performance of sensitive analog circuits. A process-invariant constant current source based on the principle of current addition has been described in [7]. Based on this principle, control circuits can be added to provide robust duty cycle under PVT variations over a wide frequency range [5]-[6]. This principle has been used in the proposed

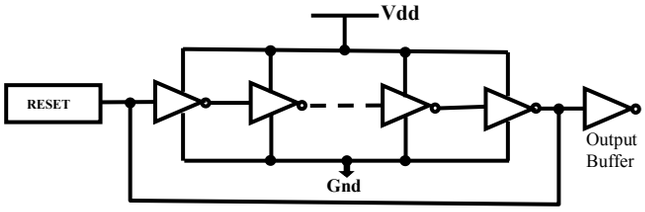

Fig. 1. Conventional ring oscillator circuit.

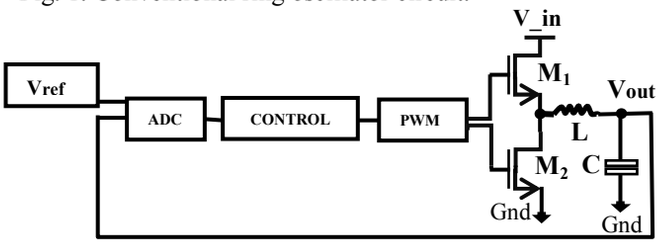

Fig. 2. Typical DC-DC inductance based switching regulator.

PWM circuit.

Utilizing a ring oscillator as a PVT-stable frequency source has been described in [10]-[13]. PVT compensations in these designs are either based on a band gap reference (BGR) or a sophisticated proportional to absolute temperature (PTAT) circuit that requires additional chip area.

An application of PWM is shown in Fig. 2 for an inductive switching DC-DC voltage converter [8]-[9]. This circuit senses the DC-DC converter analog output (*Vout*) and converts this voltage to a digital signal with the analog to digital converter (ADC) block. The digital signal is processed with a control algorithm (CONTROL) that converts the signal into a pulse width modulated form. The pulse width modulated signal from (PWM) block is applied to pass transistors (M_1, M_2), providing a stable load current. LC filter provides a stable output voltage (*Vout*).

Voltage regulation applications require accurate control of the duty cycle and frequency of the PWM output signal under varying load and PVT conditions. Several pulse width modulator architectures and implementation schemes have been reported as a part of DC-DC converter architectures [1]-[4]. These circuits have been typically implemented off-chip. This work focuses on an adaptive PWM circuit that can be fully integrated on chip.

The rest of the paper is organized as follows. The proposed PWM architecture and working principles of the ring oscillator, header, and footer control circuits are described in Section II. Simulation results and comparisons with analytic expressions are presented in Section III. Circuit physical

characteristics and comparisons with other state-of-the-art PWMs are presented in Section IV and concluding remarks offered in Section V.

II. PULSE WIDTH MODULATOR ARCHITECTURE

An architectural level block diagram of the proposed PWM based on a ring oscillator is shown in Fig. 3. The output of the ring oscillator *CLK* is fed to the duty cycle to voltage converter (DC2V) block to generate a control signal. DC2V provides an analog control signal for the headers and footers to ensure a stable duty cycle under PVT variations. Digital control provides signals for the header and footer circuits to dynamically change the duty cycle and frequency of the ring oscillator. Details of individual blocks and operational aspects are described in the following subsections.

A. Ring Oscillator Topology

A seven stage ring oscillator [5]-[6] is used for the proposed PWM as shown in Fig. 4. The odd inverter stages 1, 3, 5, and 7 are connected to header circuit Ia and footer circuit Ic. The even inverter stages 2, 4, and 6 are connected to header circuit Ib and footer circuit Id. An increase in the source current supplied to the ring oscillator by header Ia or Ib increases the current supplied to PMOS devices within the inverters, enhancing the pull-up capability and resulting in a faster rise time at the outputs. Conversely, an increase of the sink current through the footer Ic or Id increases the current through the NMOS devices of the inverters, enhancing the pull down capability and resulting in a faster fall time at the output. The relative increase or decrease in the source and sink currents therefore changes the duty cycle and frequency of the ring oscillator output. An analysis of the effect of increasing and decreasing the current in the header and footer circuits is provided in Table I.

TABLE I

Duty Cycle and frequency changes with header and footer currents.

⇧=INCREASE ⇩= DECREASE

Header or Footer Current	Duty cycle	Frequency
Ia ⇧	⇩	⇧
Ia ⇩	⇧	⇩
Ib ⇧	⇧	⇩
Ib ⇩	⇩	⇧
Ic ⇧	⇧	⇩
Ic ⇩	⇩	⇧
Id ⇧	⇩	⇧
Id ⇩	⇧	⇩

B- PWM Control

Analytic expressions for the duty cycle and frequency in terms of headers and footers currents from [5]-[6] and listed in the analysis in Table I are summarized here. A list of parameters defined for the expressions is as follows

$\alpha = IA/IA5$, $\beta = IB/IB5$, $\gamma = IC/IC5$, and $\delta = ID/ID5$

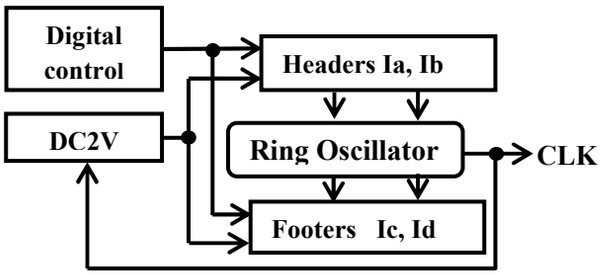

Fig. 3. Block diagram of the proposed pulse width modulator.

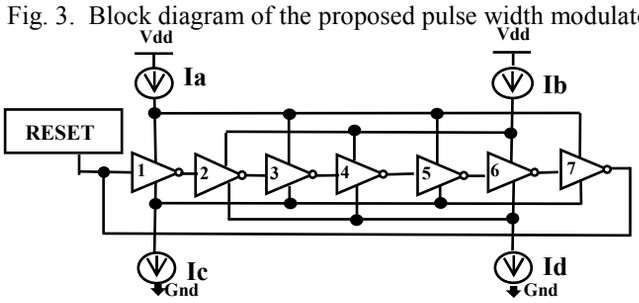

Fig. 4. Seven stage ring oscillator circuit topology.

where *IA, IB, IC* and *ID* are the currents passing through, respectively, Ia, Ib, Ic, and Id. *IA5, IB5, IC5,* and *ID5* are the currents passing through Ia, Ib, Ic, and Id respectively, to provide a 50% duty cycle.

The duty cycle and frequency of the proposed PWM are expressed as

$$D = 1/\left(1 + \frac{\alpha}{\beta} * \frac{\delta}{\gamma}\right), \quad (1)$$

$$F_{new} = 2 * (1 - D) * F_0, \quad (2)$$

where D is the duty cycle of proposed PWM, F_0 is the frequency of proposed PWM at D equal to 0.5, and F_{new} is the new frequency of the PWM. To maintain a constant frequency, the ratio of the header currents (*IB/IA*) or footer currents (*IC/ID*) is established for each value of duty cycle D as

$$IB/IA = D / (1\text{-}D), \quad (3)$$

$$IC/ID = D / (1\text{-} D). \quad (4)$$

Simulation and theoretical comparison of these equations are shown in Figs. 8, 9, and 10 and discussed in Section III.

C- Duty Cycle to Voltage Converter

The duty cycle to voltage converter (DC2V) has been adopted from [14]. A simplified diagram of the circuit is shown in Fig. 5 and has the following cycles of operation. A high *CLK* input charges capacitor C_1 from Vdd through transistor DM_0. When *CLK* goes low, a high pulse P_2 turns on DM_2 transferring charge from capacitor C_1 to C_2. After P_2 goes low while *CLK* is still low, P_1 goes high and discharges C_1 to ground through DM_1. Resistor R_1 and PMOS transistor DM_3 establish the range of *DC2VOut* voltage. After a few cycles the voltage on C_2 stabilizes to a constant value. The output of DC2V "*DC2Vout*" is used as the input "*dc2vin*" in the header and footer circuits.

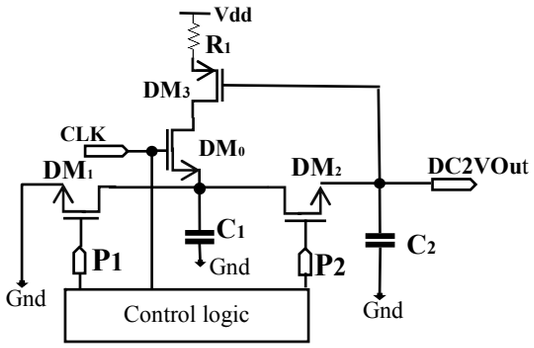

Fig. 5. Simplified schematic of DC2V.

D- Header and Footer Circuits.

The circuit schematics for headers Ia, Ib, and footers Ic, Id are shown in Figs. 6 and 7, respectively. Addition based current sources and sinks are proposed in [7] to ensure stable and robust current delivery under PVT variations. A modified addition based current source has been used within the header circuit using PMOS transistors PM_0, PM_2, PM_3, and PM_4. PMOS transistors PM_5, PM_6, and PM_7 in series with PM_2, PM_3, and PM_4 respectively control the header currents with digital inputs *bx0, bx1… bxn*. A modified addition based current sink has been used within the footer circuit using NMOS transistors NM_1, NM_3, NM_4, and NM_5. NMOS transistors NM_6, NM_7 and NM_8 in series with NM_3, NM_4, and NM_5, respectively, control the footer currents with digital input *by0, by1… byn*. The analog input *dc2vin* received from output of DC2V block provides current control for the header and footer circuits to maintain a constant current over a wide range of PVT variations. Under PVT variations, the bias voltage for transistors PM_2, PM_3, and PM_4 in the header circuit and transistors NM_3, NM_4, and NM_5 in the footer circuits respectively are adjusted to maintain current values that ensure a constant duty cycle for the PWM. Device PM_{00} and resistor RN_1 within the footer circuits provide a level shift circuit for *dc2vin*. Devices PM_0 and NM_1 within the header and footer circuits are configured as long channel devices as compared to other transistors within the header and footer circuits to mitigate leakage current variations [15].

III. SIMULATION RESULTS

The proposed PWM circuit has been implemented with 22 nm CMOS predictive technology model [16]. Simulation results of the PWM are compared with expressions defined in Section II-B. Simulation results characterizing the performance of the proposed PWM are shown in Sections III-A, B and C.

A. Digitally Controlled Variable Duty Cycle PWM

The circuit shown in Fig. 3 is simulated over a wide range of duty cycle (20-90%) by changing the digital control inputs. The results are compared with (1). Duty cycle versus normalized header and footer currents α, β, γ, and δ are shown in Figs. 8 and 9. Analytic and simulation results show good agreement within 5% of error.

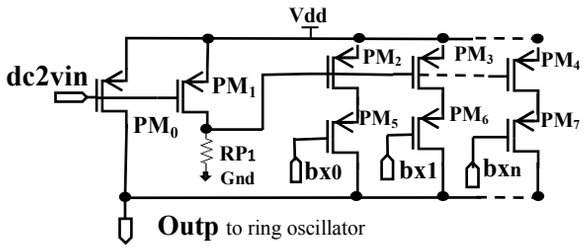

Fig. 6. Header circuit Ia or Ib. Digital inputs *bx0, bx1.. bxn* control total header current supplied through output port *Outp*.

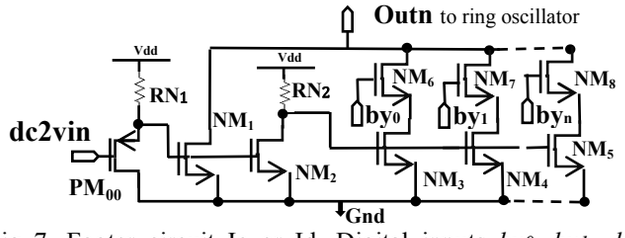

Fig 7. Footer circuit Ic or Id. Digital inputs *by0, by1.. byn* control total footer current sinking through output port *Outn*.

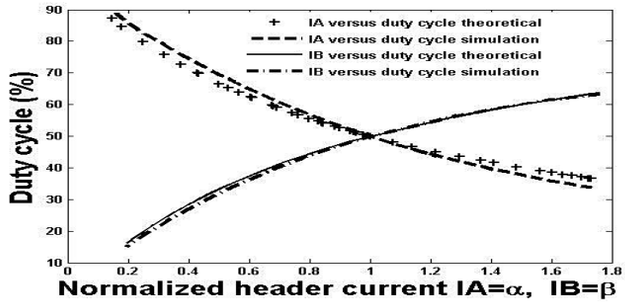

Fig. 8. Duty cycle varies between 20% and 90% with header current *IA*, *IB* variation. Theoretical versus simulation plot.

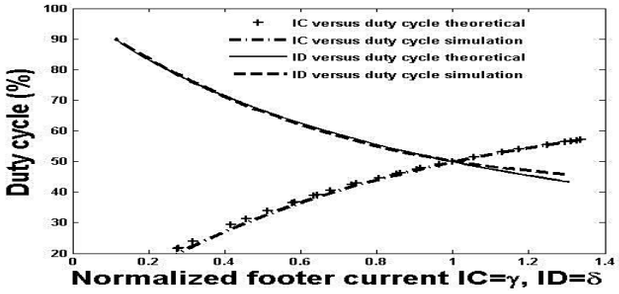

Fig. 9. Duty cycle varies between 20% and 90% with footer current *IC*, *ID* variations. Theoretical versus simulation plot.

B. Digitally Controlled Constant Frequency PWM

The ratio of the header currents *IB* to *IA* is changed to achieve a constant frequency of 1.66 GHz, over a wide range of duty cycles. Header current ratio *IB/IA* versus duty cycle and frequency with and without frequency compensation are shown in Fig. 10. Theoretical duty cycle and frequency plots based on (2) and (3) defined in Section II-B are also shown. The discrepancy between the theory and simulation is based on dynamic current ratios versus static current ratios used in (2) and (3).

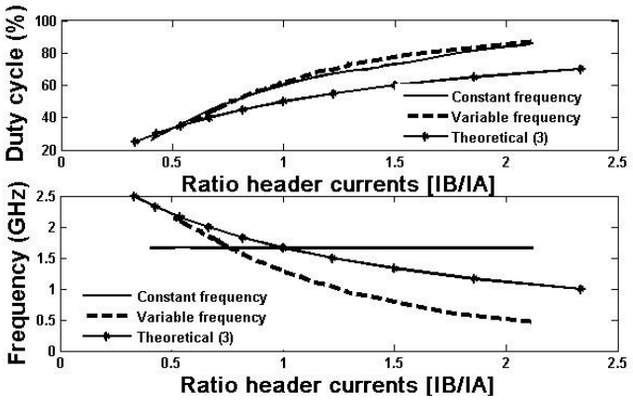

Fig. 10. Constant frequency simulation and theoretical comparison.

C. PVT Compensated PWM

The robustness of proposed PWM under PVT variations has been analyzed for a duty cycle range of 20-90%. The results are listed in Table II and demonstrate a worst case error of less than 1% for duty cycle values between 50-90% [5]-[6].

TABLE II

PROCESS (P) SS= slow, FF= Fast, TT=Typical,
VOLTAGE (V) = 0.9V – 1V, TEMP (T) = 27 °C - 80 °C
*Process parameters generated as specified in [14]-[15].

P/V/T	Duty cycle (%)							
TT/1V/27	90.00	80.00	70.00	60.00	50.00	40.00	30.00	20.00
TT/1V/80	90.32	80.27	69.54	59.77	49.91	40.05	29.61	19.58
FF/1V/27	89.83	79.64	69.91	60.08	50.04	39.56	29.52	19.43
FF/1V/80	90.27	79.77	69.54	59.55	49.97	39.53	29.10	19.97
SS/1V/27	90.01	80.29	70.09	60.03	50.03	40.37	30.45	20.23
SS/1V/80	90.30	80.50	70.14	59.70	50.12	40.49	30.22	19.91
TT/0.9V/27	89.60	79.77	69.40	59.48	49.99	40.57	31.20	21.09
TT/0.9V/80	89.89	79.97	69.47	59.51	50.08	40.73	31.00	19.98
FF/0.9V/27	89.56	79.38	69.20	59.40	49.95	40.15	30.67	20.88
FF/0.9V/80	89.84	79.48	69.10	59.18	49.69	40.15	30.22	20.48
SS/0.9V/27	90.11	79.98	69.46	59.54	50.16	41.07	32.00	21.65
SS/0.9V/80	89.84	80.22	69.60	59.70	50.11	41.26	31.80	21.32

IV. PERFORMANCE SUMMARY

A comparison of the proposed PWM with state-of-the-art PWMs is provided in Table III. The proposed PWM can be implemented in a small area and consumes significantly less power over a wide frequency range.

TABLE III

AREA, POWER AND FREQUENCY OF OPERATION COMPARED

Design	Area	Power/Frequency	Technology (CMOS)
[3]	5.52 mm^2	10.5 uW/330 KHz	0.60 um
[9]	1.00 mm^2	11.2 mw/1.25 GHz	0.13 um
[10]	1.20 mm^2	19.2 mW/2.4 GHz	0.25 um
[11]	3.20 mm^2	1.0 mW/200 KHz	0.35 um
[12]	2.00 mm^2	0.15 mW/278 MHz	65 nm
This work*	0.6 mm^2	0.2 mW/1.66 GHz, 16 uW (DC)	22 nm

- Estimated area=device area x 5, power=simulation estimate.

V. CONCLUSIONS

A digitally controlled PWM has been proposed that adaptively changes the header and footer current profiles to maintain a constant duty cycle under PVT variations. The proposed circuit can adaptively control the duty cycle and the frequency at runtime. A DC2V converter and novel header and footer circuits are employed to achieve a stable duty cycle operation under PVT variation. The proposed footer and header circuits improve the error margin of duty cycle variations over a wide PVT range.

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