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Efficient algorithms for fast *IR* drop analysis exploiting locality

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ABSTRACT

Closed-form expressions and related algorithms for fast power grid analysis are proposed in this paper. Four algorithms to determine the *IR* voltage drop at an arbitrary node are described when voltage supplies and current loads are non-uniformly distributed throughout a power grid. Two techniques are used to determine the effective impedance in a non-uniform and semi-uniform power grid. An effective resistance model is proposed for semi-uniform power grids. The principle of spatial locality is exploited to accelerate the proposed power grid analysis process. Since no iterations are required for the proposed *IR* drop analysis, the proposed algorithms are over 60 and two times faster for smaller power grids composed of less than five million nodes and over 175 and three times faster for larger power grids composed of more than 25 million nodes as compared to, respectively, the random walk and second order iterative methods. The proposed method exhibits less than 0.3% error.

1. Introduction

With reduced power supply levels in modern microprocessors, *IR* drop analysis has become a crucial part of the circuit design process since the performance of each individual circuit block depends upon the voltage within the power distribution network [1–3]. Efficient analysis of the *IR* drops, however, is a difficult task due to the large physical dimensions of the power distribution network and the complex global interactions among the loads.

The *IR* drop analysis process can be formulated as a linear system with a conductance matrix modeling the power grid impedance. This matrix is solved by assigning a source vector for the voltage sources and another vector for the current loads. Although the formulation of the *IR* drop analysis process is straightforward, the solution of this linear system is infeasible for a typical power distribution network due to the large size. For example, if the power distribution system is composed of N rows and N columns, the total number of nodes is N^2, and the resulting conductance matrix to solve this power distribution network is $N^2 \times N^2$ [4]. The size of the conductance matrix therefore increases quadratically with increasing size of the power network. Due to the large size of power distribution networks in modern high complexity circuits, traditional linear solvers are incapable of solving this large linear system in reasonable time.

Several methods have been proposed for efficient power grid analysis; (1) reduce the size of the linear system, (2) iteratively solve the linear system, and (3) apply advanced linear algebraic techniques to exploit the sparse nature of the power grid. Conventional interconnect model order reduction techniques [5] are applicable for tree structured interconnects; however, these methods are inappropriate for mesh structured power distribution networks. The power grid can be reduced to a simpler structure where this coarse structure is later mapped into the original grid [2]. The power grid is optimized to minimize the *IR* drop at the grid center in [6]. In [7], the power grid is partitioned into a number of smaller parts where each partition is analyzed separately. Random walk techniques are used to analyze a power grid in [8] to iteratively solve the *IR* drop problem without computing large matrix operations. In [9], the power supply network is analyzed using stochastic voltage prediction. Efficient first and second order iterative algorithms are proposed, respectively, in [4,10]. Although these algorithms are faster than conventional linear solvers, significant computational time is required to iteratively apply these algorithms. An accurate closed-form expression would effectively solve this problem.

Although the interactions between the power supplies and load circuitry occur globally, these interactions are more prominent among components in close proximity [1,11–13]. Within a single integrated circuit (IC), a power supply connection in a multi-voltage system on one side of an IC has little effect on a circuit block at the other side of the IC. Alternatively, current provided by a power network is generally distributed to nearby circuit blocks. This phenomenon is due to the principle of spatial locality [11]. With this principle, a power grid can be partitioned to enhance the power grid analysis process.

Uniform current loads are generally assumed in power distribution networks to exploit symmetry in a linear system. In [14],

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an *IR* drop analysis algorithm is described for a power grid structure with semi-uniform current loads (*e.g.*, uniform load currents are assumed within each quadrant of the distribution network). Closed-form expressions for the maximum *IR* drop are described in [15], assuming a uniform current distribution. To the authors' knowledge, the results published here are the first closed-form expressions that describe the voltage drop at any node in a power distribution network with non-uniform current loads and non-uniform voltage supplies.

In this paper, closed-form expressions for estimating the *IR* drop in a power grid with non-uniform current loads and non-uniform voltage supplies are provided. The proposed method exploits the impedance characteristics of the power distribution network and the effective impedance among the active circuit blocks to provide these closed-form expressions. The effective resistance between two nodes in an infinite uniform resistive network and non-uniform finite resistive network has been considered by, respectively, Venezian [16] and Wu [17]. In this paper, the closed-form expression in [16] is generalized to consider semi-uniform power grids where the horizontal and vertical resistances are different. Since no iterations are required to compute the *IR* drop at any particular node, the proposed algorithm outperforms previously proposed techniques with small error. The principle of locality is also applied in this algorithm to accelerate the analysis process.

The rest of the paper is organized as follows. The power grid model is described and the *effective resistance* concept is explained in Section 2. In Section 3, the proposed algorithm is reviewed for different conditions. The principle of spatial locality is further explained and exploited to accelerate the proposed power grid analysis process in Section 4. Experimental results are provided in Section 5. The paper is summarized in Section 6, followed by a derivation of the closed-form expression for the effective resistance in the Appendix.

2. Background

In this section, closed-form expressions for the *IR* voltage drop are described that exploit the distance between the voltage sources and current loads. The *IR* voltage drop at an arbitrary node depends upon the distance among the voltage sources, current loads, and analysis nodes. These distances are incorporated into the closed-form expressions by the concept of an effective resistance since the effective resistance between any two nodes in a uniform grid structure depends upon the euclidean distance between these two nodes and the power grid resistance. The concept of an effective resistance supports the development of closed-form expressions for use within the power grid analysis process.

A two layer power/ground network is shown in Fig. 1a where the dark and light grey lines illustrate, respectively, the power and ground lines. The power network and corresponding circuit model are shown, respectively, in Fig. 1b and c. Since this paper focuses on resistive voltage drop analysis, only a resistive network is considered although inductance could easily be included. Effective resistance models for two different power grids are considered in this paper. First, the effective resistance in a non-uniform power grid [17] is considered by utilizing Green's function. The effective resistance between nodes m and n is

$$R_{m,n} = \sum_{i=2}^{N} \frac{1}{\lambda_i} |\psi_{im} - \psi_{in}|, \tag{1}$$

where $\boldsymbol{\lambda_i}$ is the nonzero eigenvalues and $\boldsymbol{\psi_i} = (\psi_{i_1}, \psi_{i_2}, \ldots, \psi_{i_N})$ are the orthonormal eigenvectors of the corresponding Kirchhoff matrix.

When the power distribution model consists of vertical and horizontal lines with, respectively, resistances r_v and r_h, the effective resistance is described by Venezian in [16] when $r_v = r_h$. In this work, a more general effective resistance model is proposed where $r_h = k * r_v$, as illustrated in Fig. 1c. The assumption $r_h = k * r_v$ is a reasonable approximation in modern integrated circuits during localized analysis of power grids [18–20].

An exact solution for the effective resistance between any two points, $N_1(x_1, y_1)$ and $N_2(x_2, y_2)$, is

$$R_{x,y} = \frac{kr}{\pi} \int_0^{\pi} \frac{2 - e^{-|x|\alpha} \cos y\beta}{\sinh \alpha} \, d\beta \tag{2}$$

and the closed-form approximation for (2) is

$$R_{x,y}/r = \frac{\sqrt{k}}{2\pi} * \ln(x^2 + ky^2) + 3.44388 - 0.0033425k - \frac{0.1975k(k-1)}{\pi}, \tag{3}$$

where

$$x = |x_1 - x_2|, \tag{4}$$

$$y = |y_1 - y_2|, \tag{5}$$

$$r_v = r, \tag{6}$$

$$r_h = k * r. \tag{7}$$

α and β are used to rewrite Kirchhoff's node equations as difference equations satisfying $k + 1 = k \cos \beta + \cosh \alpha$ and r is the unit resistance. A derivation of the closed-form approximation of the effective resistance is provided in the Appendix.

While (1) provides an exact solution for the effective resistance in a non-uniform power grid, (3) provides an efficient approximate solution for a semi-uniform power grid. The error of (3) is less than 3%, as listed in Table 1 [16]. A few examples that demonstrate the validity of (3) are listed in Table 1 when $k = 1$. The error quickly approaches zero with increasing distance between two points. For instance, the average error when determining all of the resistances in a 50×50 grid is less than 0.01%. Power grids in modern integrated circuits generally exhibit a locally uniform, globally non-uniform structure. Eq. (3) can be used when the power

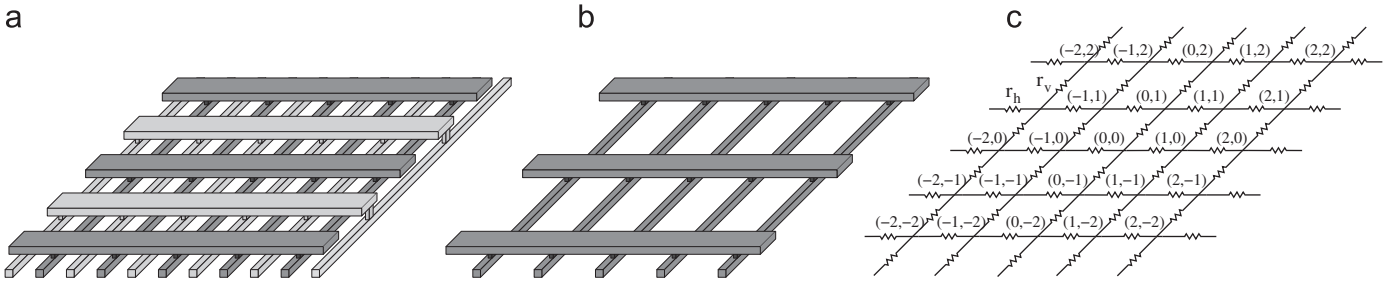

Fig. 1. Two layer orthogonal metal lines connected with vias; (a) two layer power and ground distribution networks where the power and ground lines are illustrated, respectively, with dark and light grey, (b) a two layer power distribution network, and (c) a resistive mesh model of the power distribution network.

grid exhibits a semi-uniform structure to reduce the computational time of the power grid analysis process. Alternatively, when the power grid exhibits a non-uniform structure, (1) can be used to determine the effective resistance. The runtime of the proposed algorithm is, however, significantly slower for non-uniform power grids. Since a partitioning based approach is utilized in this paper, the runtime can be improved by utilizing (3) for uniform partitions and (1) for non-uniform partitions.

3. Analytic *IR* drop analysis

Four different algorithms are described in this section to determine the *IR* drop at an arbitrary node within a uniform power grid:

- Algorithm I: One power supply and one current load placed arbitrarily within the distribution network.
- Algorithm II: One power supply and multiple current loads placed arbitrarily within the distribution network.
- Algorithm III: Multiple power supplies and one current load placed arbitrarily within the distribution network.
- Algorithm IV: Multiple power supplies and multiple current loads placed arbitrarily within the distribution network.

Table 1
Validity of the effective resistance model.

	$R_{1,0}$	$R_{1,1}$	$R_{3,4}$	$R_{5,0}$	$R_{10,10}$
Exact solution (2)	0.5	0.636	1.028	1.026	1.358
Approximation (3)	0.515	0.625	1.027	1.027	1.358
Error (%)	3	1.8	0.1	0.1	0

A simplified model to demonstrate these four cases is illustrated in Fig. 2. The voltage supplies and current loads are illustrated as V_{supply} and I_{load}. Algorithm I is the most basic algorithm and is therefore used to explain the other three algorithms. Algorithm IV is the complete algorithm which can be used in the analysis of *IR* drops within practical power grids. The distance between two nodes does not affect the computational complexity of determining the effective resistance between these nodes. The computational complexity of the proposed algorithms to determine the *IR* drop at an arbitrary node does not therefore depend upon the size of the power grid.

3.1. One power supply and one current load

In this section, the *IR* voltage drop at an arbitrary node Node_1, shown in Fig. 3a, is determined when one power supply and one current load exist within the power grid. The power grid model, shown in Fig. 3a, reduces to an effective resistance model to determine the voltages at N_{load} and Node_1, as illustrated, respectively, in Fig. 3b and c. The effective resistance between N_{supply} and Node_1, Node_1 and N_{load}, and N_{supply} and N_{load} is denoted, respectively, as R_{sn}, R_{nl}, and R_{sl}. These effective resistances are determined with either (1) or (3) depending upon the power grid characteristics, as discussed in Section 2.

The voltage at N_{load} is

$$V_{load} = V_{supply} - I_{load} * R_{sl}. \tag{8}$$

After determining the voltage at N_{load} (see Fig. 3a), the voltage at Node_1 can be found using the principle of superposition for the

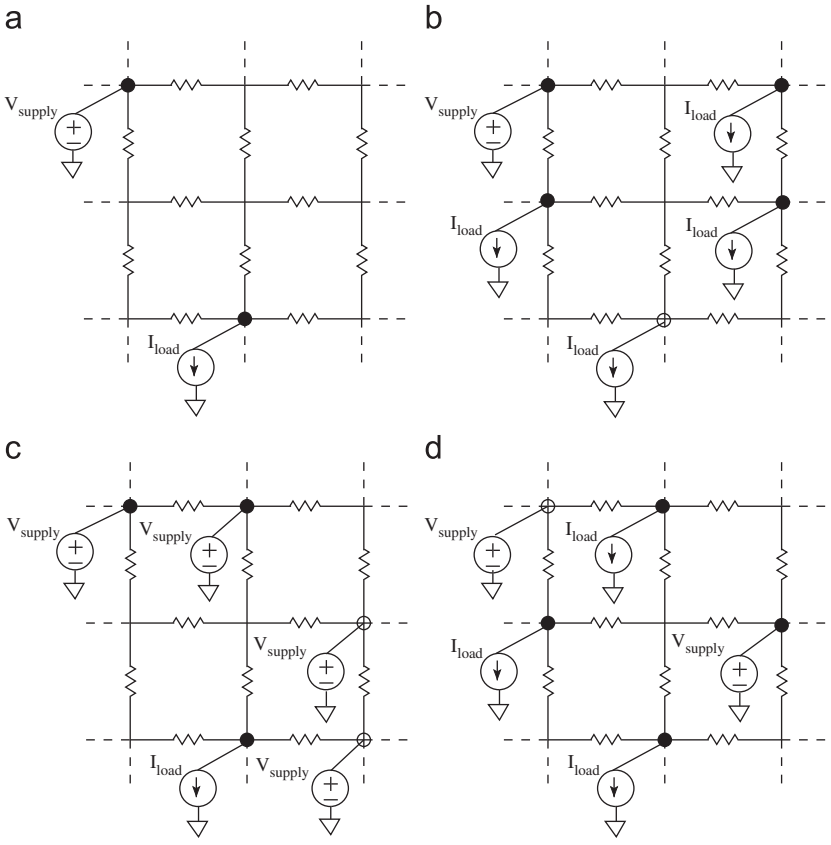

Fig. 2. Simplified power grid models with (a) one voltage source and one current load, (b) one voltage source and multiple current loads, (c) multiple voltage sources and one current load, and (d) multiple voltage sources and multiple current loads.

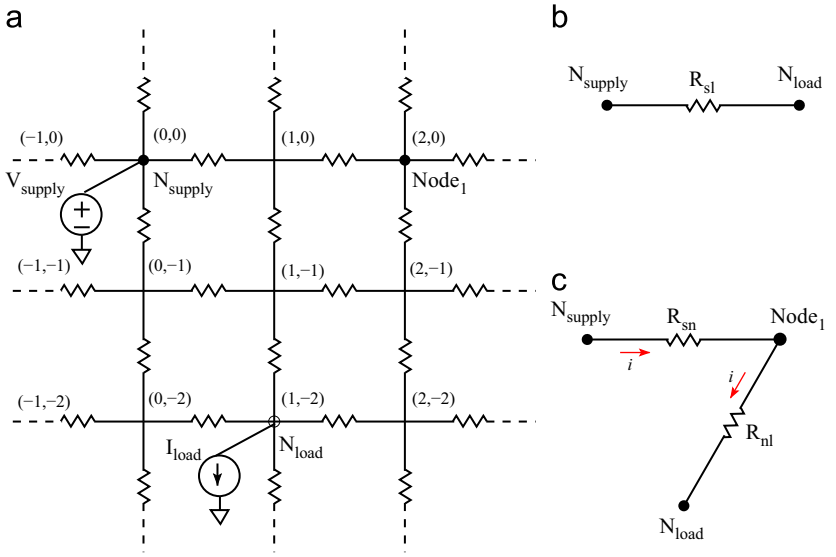

Fig. 3. Power distribution grid model: (a) one power supply connected at (0,0) and one current load connected at $(1,-2)$, (b) corresponding reduced effective resistance model between the power supply and the load, and (c) the effective resistance model to determine the voltage at an arbitrary node Node_1 within the power grid.

effective resistance model illustrated in Fig. 3c

$$V_{Node_1} = V_{supply} * \frac{R_{nl}}{R_{sn}+R_{nl}} + V_{load} * \frac{R_{sn}}{R_{sn}+R_{nl}}. \tag{9}$$

Assuming the current i, depicted in Fig. 3, is

$$i = \frac{V_{supply} - V_{load}}{R_{sn}+R_{nl}} \tag{10}$$

and substituting (10) into (9), the voltage at Node_1 is

$$V_{Node_1} = [V_{supply} + V_{load} + i*(R_{nl} - R_{sn})]/2. \tag{11}$$

Assuming $i = I_{load}$ and substituting (8) into (11), the voltage at Node_1 is

$$V_{Node_1} = [2*V_{supply} + I_{load}*(R_{nl} - R_{sn} - R_{sl})]/2. \tag{12}$$

The *IR* voltage drop at Node_1 is equal to $V_{supply} - V_{Node_1}$. The *IR* voltage drop can therefore be written as

$$IR_{Node_1} = I_{load}*(R_{sn} + R_{sl} - R_{nl})/2. \tag{13}$$

Pseudo-code of the algorithm to determine the voltage at an arbitrary node within a power grid with one current load and one power supply is summarized in Fig. 4 (Algorithm I).

IR Drop: One Power Supply and One Current Load
1. Given: Supply voltage (V_{supply}), load current (I_{load})
   Locations of voltage supply (N_{supply}),
   current load (N_{load}), and Node_1.
2. Calculate the effective resistances between
   a) N_{supply} and Node_1, R_{sn}
   b) Node_1 and N_{load}, R_{nl}
   c) N_{supply} and N_{load}, R_{sl}.
3. Calculate the voltage at N_{load}, (8).
4. Calculate the voltage at Node_1 V_{Node_1}, (11).
5. Calculate the *IR* drop at Node_1, (13).

Fig. 4. Algorithm I. *IR* voltage drop at an arbitrary node within a power grid with one power supply and one current load.

3.2. One power supply and multiple current loads

In this section, the *IR* voltage drop at an arbitrary node within a power distribution network is determined when one power supply and multiple current loads exist within a grid (see Fig. 5). Since the current loads are assumed to be ideal current sources, the principle of superposition is applied to provide a closed-form expression for the *IR* voltage drop. Superposition is possible since linear current loads are used to model the active circuit structures. By applying superposition for each individual current load, the voltage at Node_1 can be formulated as

$$V_{Node_1} = V_{supply} - \frac{1}{2}\sum_{i=1}^{n}[I_{load(i)} * (R_{sn} + R_{sl(i)} - R_{nl(i)})] \tag{14}$$

and the corresponding *IR* voltage drop at Node_1 is

$$IR_{Node_1} = \frac{1}{2}\sum_{i=1}^{n}[I_{load(i)} * (R_{sn} + R_{sl(i)} - R_{nl(i)})], \tag{15}$$

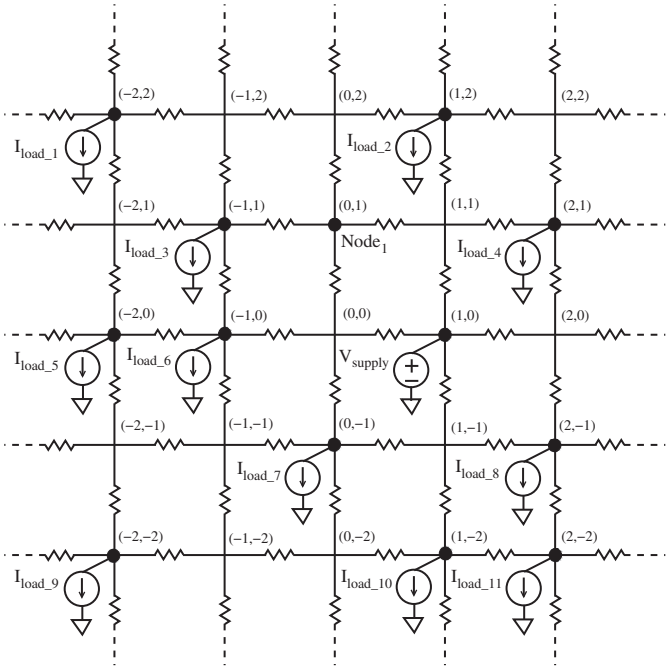

Fig. 5. Model of power distribution grid when one power supply is connected to node (1,0) and multiple current loads model the load circuits connected at various nodes within the power distribution grid.

where n is the number of current loads, $I_{load(i)}$ is the ith current load, $R_{sl(i)}$ is the effective resistance between the N_{supply} and the ith current load, and $R_{nl(i)}$ is the effective resistance between $Node_1$ and the ith current load within the power grid. Pseudo-code of the algorithm to determine the *IR* voltage drop at an arbitrary node when one voltage supply and multiple current loads are connected to a power distribution grid is provided in Fig. 6 (Algorithm II).

3.3. Multiple power supplies and one current load

In this section, the *IR* voltage drop at an arbitrary node within a power distribution network is determined for multiple voltage sources and one current load, as shown in Fig. 7a. In Section 3.2, superposition is used to analyze the voltage drop contribution to $Node_1$ from each individual current load. In a system with multiple voltage supplies, superposition cannot be applied in a straightforward manner to individually consider each voltage supply because the voltage supplies are replaced with short circuit equivalents whereas the current loads are replaced with open circuit equivalents.

The voltage supplies are replaced with equivalent current sources to apply superposition. The current that each individual voltage source contributes to the load depends upon the effective resistance between $N_{supply(i)}$ and N_{load}. Since the location of the voltage supplies and the current load is known *a priori*, the current delivered by these equivalent current supplies is approximately

$$I_{source}(i) = I_{load} * \frac{G_i}{\sum_{i=1}^{n} G_i}, \tag{16}$$

where $I_{source(i)}$ is the equivalent current source to replace the ith voltage supply and G_i is the equivalent conductance between the ith voltage supply and the current load. After all but one of the voltage supplies are replaced with equivalent current sources, as illustrated in Fig. 7b, the *IR* voltage drop problem becomes similar to the problem discussed in Section 3.2 where the power grid has one voltage supply and multiple current loads. The primary difference is that the equivalent current sources supply current to the distribution grid whereas, as described in Section 3.2, all of the current loads demand current from the power grid.

The *IR* voltage drop at an arbitrary node $Node_1$ in the power grid with multiple voltage sources and one current load is

$$IR_{Node_1} = I_{load} * (R_{sn(1)} + R_{sl(1)} - R_{nl})/2 - \frac{1}{2}\sum_{i=2}^{n}[I_{supply(i)} * (R_{sn(1)} + R_{sl(i)} - R_{nl(i)})] \tag{17}$$

and the voltage at $Node_1$ is

$$V_{Node_1} = V_{supply(1)} - I_{load} * (R_{sn(1)} + R_{sl(1)} - R_{nl})/2 + \frac{1}{2}\sum_{i=2}^{n}[I_{supply(i)} * (R_{sn(1)} + R_{sl(i)} - R_{nl(i)})]. \tag{18}$$

Pseudo-code of the algorithm to determine the *IR* voltage drop at an arbitrary node within a power grid with multiple voltage supplies and one current load is summarized in Fig. 8 (Algorithm III).

IR Drop: One Power Supply and Multiple Current Loads
1. Given: Supply voltage (V_{supply}), load currents ($I_{load(i)}$)
   Locations of voltage supply (N_{supply}),
   current loads ($N_{load(i)}$), and $Node_1$.
2. **for** each current load, $I_{load(i)}$, **do**
3. Remove all other $I_{load(k)}$ where k≠i,
4. Calculate the effective resistances between
   a) N_{supply} and $Node_1$, R_{sn}
   b) $Node_1$ and $N_{load(i)}$, $R_{nl(i)}$
   c) N_{supply} and $N_{load(i)}$, $R_{sl(i)}$.
5. Calculate the voltage at $N_{load(i)}$, (8).
6. Calculate the *IR* drop at $Node_1$ due to $I_{load(i)}$, (13).
7. Calculate the total *IR* drop at $Node_1$ by summing all *IR* voltage drops due to all individual current loads, (15).
8. Calculate the voltage at $Node_1$, V_{node_1}, (14).

Fig. 6. Algorithm II. *IR* voltage drop at arbitrary node $Node_1$ within a power grid with one power supply and multiple current loads, as shown in Fig. 5.

3.4. Multiple power supplies and multiple current loads

In this section, the *IR* voltage drop at an arbitrary node within a power distribution network is determined when multiple voltage supplies and multiple current loads exist, as shown in Fig. 9a. To determine the *IR* voltage drop for this system, superposition is applied in two steps. First, the current that each individual voltage

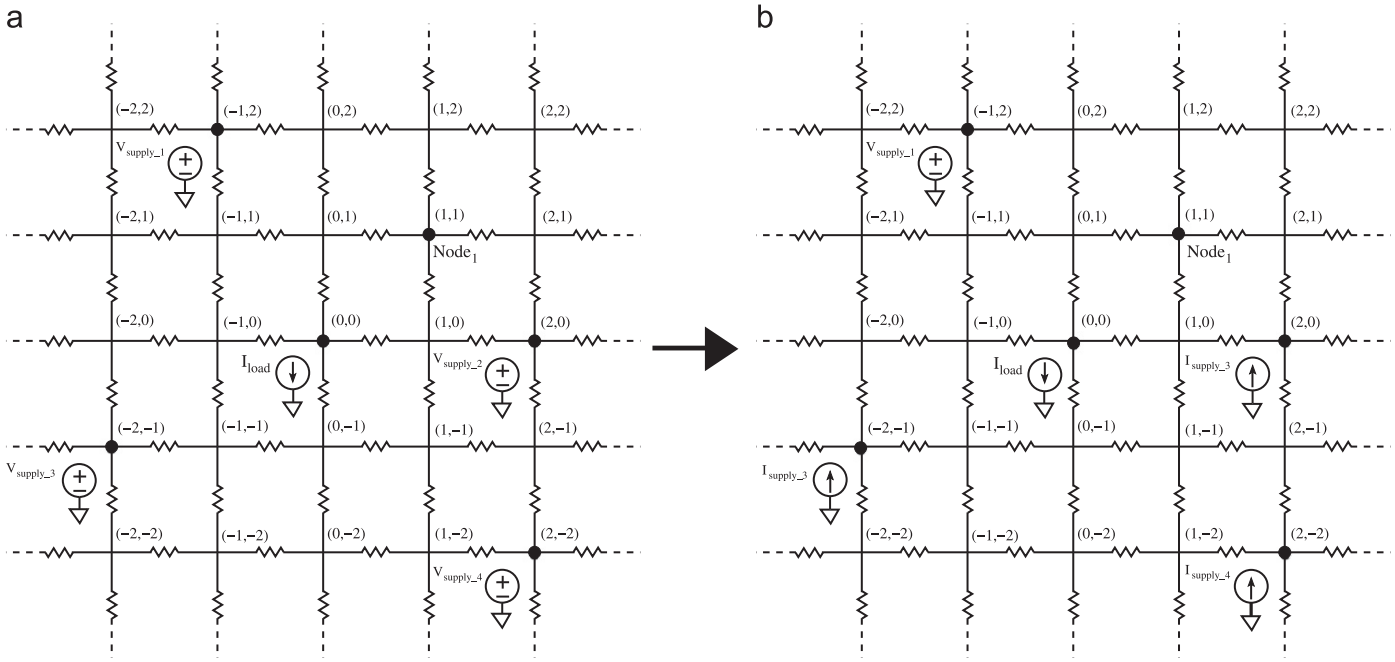

Fig. 7. Power distribution grid model: (a) multiple power supplies are connected to several nodes and a current load is connected at (0,0) and (b) all but one of the voltage sources are replaced with an equivalent current source.

supply contributes to each individual current load is determined by removing all but one of the current loads and applying (16) to determine the current contribution of each voltage supply to each current load. After determining the individual current contributions, the equivalent current source of a voltage supply is

$$I_{source}(i) = \sum_{j=1}^{m} I_{source(i,j)}, \tag{19}$$

where m is the number of current loads, $I_{source(i)}$ is the equivalent current source of the ith voltage supply, and $I_{source(i,j)}$ is the current contribution of the ith voltage supply to the jth current load. Since the total current sourced by the voltage supplies is equal to the total current sunk by the current sources, the following expression is satisfied:

$$\sum_{i=1}^{n} I_{source}(i) = \sum_{j=1}^{m} I_{load(j)}. \tag{20}$$

All but one of the voltage supplies are replaced with an equivalent current source, as illustrated in Fig. 9b. The *IR* voltage drop at an arbitrary node within a power distribution network is

$$IR_{Node_1} = \frac{1}{2}\sum_{i=1}^{m}[I_{load(i)} * (R_{sn(1)} + R_{sl(1)} - R_{nl})] - \frac{1}{2}\sum_{i=2}^{n}[I_{supply(i)} * (R_{sn(1)} + R_{sl(i)} - R_{nl(i)})] \tag{21}$$

and the corresponding voltage at $Node_1$ is

$$V_{Node_1} = V_{supply(1)} - \frac{1}{2}\sum_{i=1}^{m}[I_{load(i)} * (R_{sn(1)} + R_{sl(1)} - R_{nl})] + \frac{1}{2}\sum_{i=2}^{n}[I_{supply(i)} * (R_{sn(1)} + R_{sl(i)} - R_{nl(i)})], \tag{22}$$

where m is the number of current loads and n is the number of voltage supplies. Pseudo-code of the algorithm to determine the *IR* voltage drop at an arbitrary node for multiple voltage supplies and current loads is provided in Fig. 10 (Algorithm IV).

IR Drop: Multiple Power Supplies and One Current Load
1. Given: Supply voltage (V_{supply}), load current (I_{load})
   Locations of voltage supplies ($N_{supply(i)}$),
   current load (N_{load}), and $Node_1$.
2. **for** each voltage supply, $V_{supply(i)}$, **do**
3. Calculate the effective resistances between $N_{supply(i)}$ and I_{load}, R_i.
4. **for** each voltage supply, $V_{supply(i)}$, where i≠1, **do**
5. Find the corresponding current source, $I_{supply(i)}$, (16).
6. Replace $V_{supply(i)}$ with $I_{supply(i)}$.
7. Remove all current supplies, $I_{supply(i)}$.
8. Calculate the effective resistances between
   a) $N_{supply(1)}$ and $Node_1$, R_{sn}
   b) $Node_1$ and N_{load}, R_{nl}
   c) $N_{supply(1)}$ and N_{load}, R_{sl}.
9. Calculate the *IR* drop at $Node_1$ due to I_{load}, (13).
10. **for** each current supplies, $I_{supply(i)}$, **do**
11. Remove all other current supplies, $I_{supply(k)}$, where k≠1.
12. Calculate the effective resistances between
   a) $N_{supply(1)}$ and $Node_1$, R_{sn}
   b) $Node_1$ and $N_{supply(i)}$, $R_{nl(i)}$
   c) $N_{supply(1)}$ and $N_{supply(i)}$, $R_{sl(i)}$.
13. Calculate the voltage difference at $Node_1$ due to $I_{supply(i)}$, (13).
14. Calculate the total *IR* drop at $Node_1$ by subtracting the result of step 13 from the result of step 9, (17).
15. Calculate the voltage at $Node_1$, V_{node_1}, 18.

Fig. 8. Algorithm III. *IR* voltage drop at arbitrary node $Node_1$ in a power grid with multiple power supplies and one current load, as shown in Fig. 7(a).

4. Locality in power grid analysis

Practical power grids in high performance integrated circuits can be treated as locally uniform, globally non-uniform resistive meshes. To apply these algorithms to the analysis of practical power grids, the principle of spatial locality [1,11–13,21] is applied. This principle for a resistive power grid is described in Section 4.1. The effect of utilizing spatial locality on the power grid analysis process is explained in Section 4.2. In Section 4.3, the principle of spatial locality is exploited and integrated into this power grid analysis method. The advantages of utilizing spatial locality in the power grid

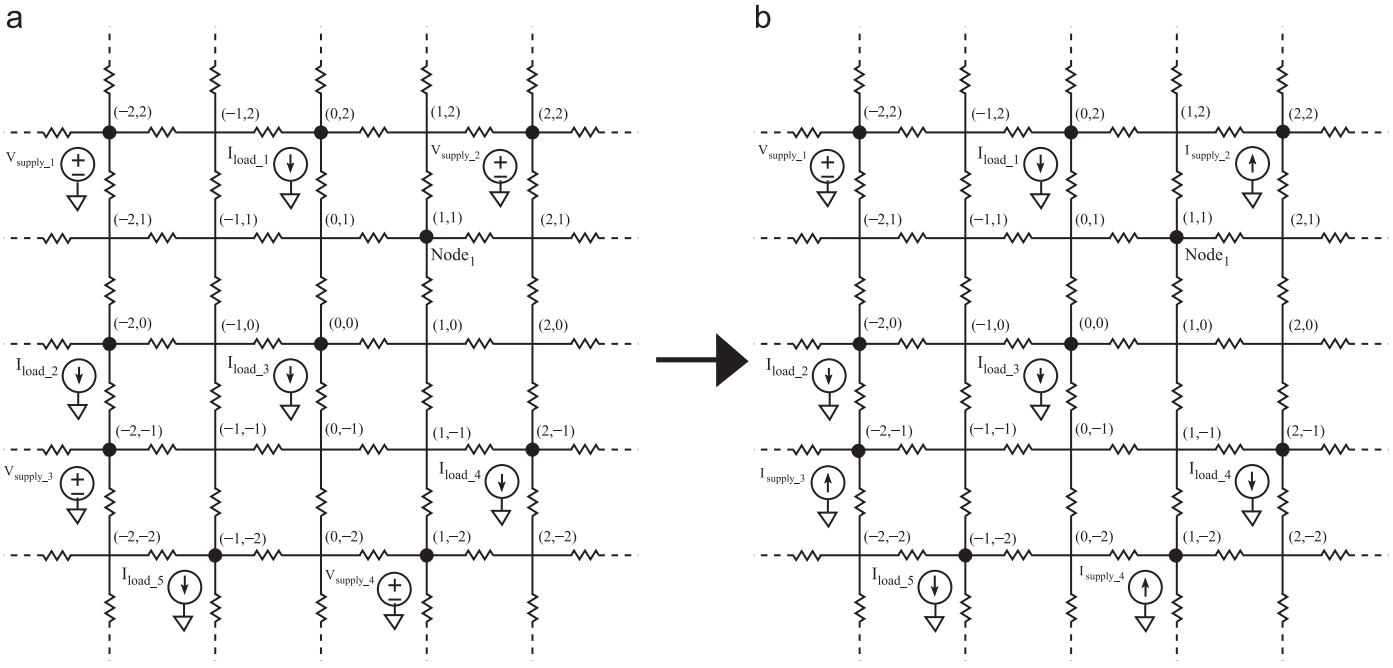

Fig. 9. Power distribution grid model (a) multiple power supplies and current loads are connected to several nodes and (b) all but one of the voltage sources are replaced with an equivalent current source.

IR Drop: Multiple Power Supplies and Multiple Current Loads
1. Given: Supply voltage (V_{supply}), load currents ($I_{load(j)}$)
   Locations of voltage supplies ($N_{supply(i)}$),
   current loads ($N_{load(j)}$), and $Node_1$.
2. **for** each voltage supply, $V_{supply(i)}$, **do**
3. **for** each current load, $I_{load(j)}$, **do**
4. Calculate the effective resistances between
   $N_{supply(i)}$ and $I_{load(j)}$, $R_{(i,j)}$.
5. **for** each voltage supply, $V_{supply(i)}$, where $i \neq 1$, **do**
6. **for** each current load, $I_{load(j)}$, **do**
7. Find the corresponding current, $I_{supply(i,j)}$, (16).
8. Sum up $I_{supply(i,j)}$ for all j to calculate $I_{supply(i)}$, (19).
9. Replace $V_{supply(i)}$ with $I_{supply(i)}$.
10. **for** each current load, $I_{load(j)}$, **do**
11. Remove all current supplies, $I_{supply(i)}$.
12. Calculate the effective resistances between
    a) $N_{supply(1)}$ and $Node_1$, R_{sn}
    b) $Node_1$ and $N_{load(j)}$, $R_{nl(j)}$
    c) $N_{supply(1)}$ and $N_{load(j)}$, $R_{sl(1,j)}$.
13. Calculate the *IR* drop at $Node_1$ due to all $I_{load(j)}$, (13).
14. **for** each current supply, $I_{supply(i)}$, **do**
15. Remove all other current supplies, $I_{supply(k)}$, where $k \neq 1$.
16. Remove all current loads, $I_{load(j)}$.
17. Calculate the effective resistances between
    a) $N_{supply(1)}$ and $Node_1$, R_{sn}
    b) $Node_1$ and $N_{supply(i)}$, $R_{nl(i)}$
    c) $N_{supply(1)}$ and $N_{supply(i)}$, $R_{sl(i)}$.
18. Calculate the voltage difference at $Node_1$ due to $I_{supply(i)}$, (13).
19. Calculate the total *IR* drop at $Node_1$ by subtracting
    the result of step 18 from the result of step 13, (21).
20. Calculate the voltage at $Node_1$, V_{node_1}, (22).

Fig. 10. Algorithm IV. *IR* voltage drop at an arbitrary node $Node_1$ within a power grid with multiple power supplies and current loads, as shown in Fig. 9a.

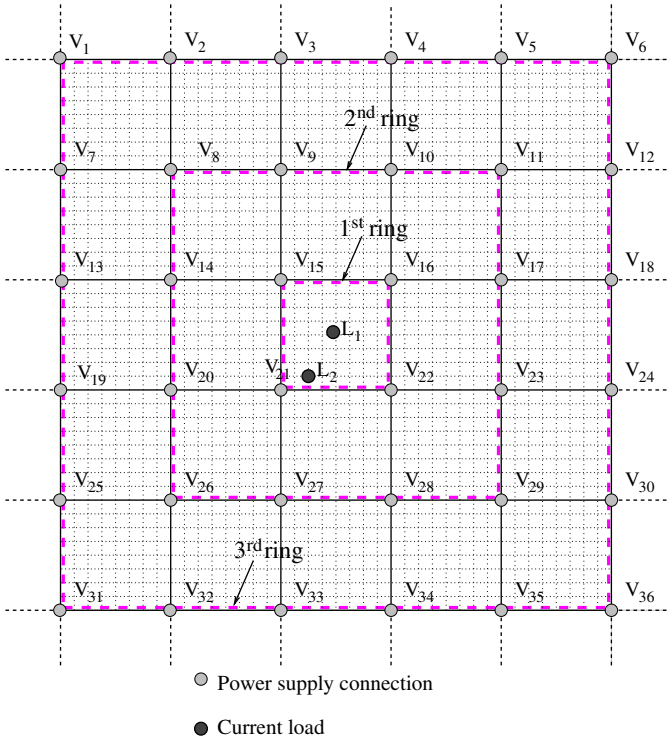

Fig. 11. A portion of a typical power grid with C4 bumps illustrated with light dots and load devices with dark dots. Most of the current sunk by the load devices, L_1 and L_2, is provided by the supply connections forming the first ring. Power supply connections within the third ring contribute less than 1% of the total current to these load devices.

analysis process are also explored. An error correction technique is introduced in Section 4.4.

4.1. Principle of spatial locality in a power grid

Flip-chip packages are widely used in high performance integrated circuits, increasing the number of voltage supply connections to the integrated circuit. Controlled collapse chip connect (C4) bumps connect the integrated circuit to external circuitry from the top side of the wafer using solder bumps. A large number of power supply connections are therefore provided to the power grid via these C4 bumps. Most of the current to the load devices is provided from those power supply connections in close proximity due to the smaller effective impedance. This phenomenon can be explained using the principle of spatial locality in a power grid [1,11–13].

A power grid for a flip-chip package with C4 connections is illustrated in Fig. 11. To exemplify the principle of spatial locality in a power grid, two current loads are connected to the power grid, as depicted in Fig. 11, to analyze the current contributions from each supply connection. With only one current load L_1 connected to the power grid, the current contributed from each of the C4 connections to L_1 is as illustrated in Fig. 12. Most of the current is provided by the close power supplies. The current contribution of a supply connection decreases significantly with distance. The current contribution from most of the supply connections within the third ring is less than 1% of the total load current. The current contribution from each supply connection is also analyzed with only the current load L_2 connected to the power grid. More than 40% of the total current is provided by the closest power supply connection, V_{21}. The current contribution of all of the connections is illustrated in Fig. 13. Most of the power supply connections within the third ring contribute less than 1% of the current to the load. When the load circuit is close to the boundary of the power supply ring, the current provided by some power supply connections within the outer ring can be higher than the current contributed by the connections forming the inner ring. For instance, since L_2 is close to the first ring boundary, the current contribution from V_{27} which is in the second ring is higher than the current contributed by V_{16} which is in the first ring. The reason is that V_{27} is physically closer to L_2 than V_{16}. The principle of locality is therefore applicable to power grids with multiple power supply connections such as flip-chip packages. Locality can also be applied to power distribution networks with tens of on-chip voltage regulators. In this case, most of the current is supplied by the closest on-chip power supplies rather than the closest C4 connections.

4.2. Effect of spatial locality on computational complexity

The computational complexity of the power grid analysis process can be significantly reduced by introducing spatial locality since the voltage fluctuations at a specific node are primarily determined by the power grid impedance and placement of those supply connections in close proximity [11]. The complex global interactions among distant circuit components, which typically have a negligible effect on the *IR* drop, is not considered with spatial locality. Additionally, the computational runtime of the power grid analysis process can be significantly reduced with parallelization [22]. Since each partition is analyzed individually in the proposed algorithm, parallelization of the proposed algorithm is straightforward.

4.3. Exploiting spatial locality in the proposed method

An infinite grid is assumed in these algorithms when using (2) to determine the effective resistance of a finite power grid. This assumption introduces an approximation error to the proposed power grid analysis process when evaluating small power grids. When the size of the power grid increases, the introduced error converges to zero. The maximum error for various grid sizes is

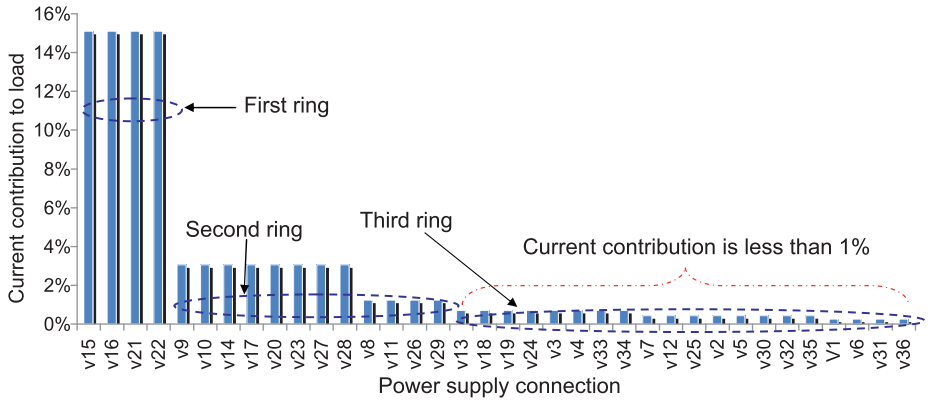

Fig. 12. Percent current provided to the current load L_1 placed in the middle of a uniform power grid from the power supplies, as illustrated in Fig. 11. Note that most of the current is provided by the power supplies within the closest two rings whereas the current provided by the power supplies within the third ring is less than 1% of the total load current.

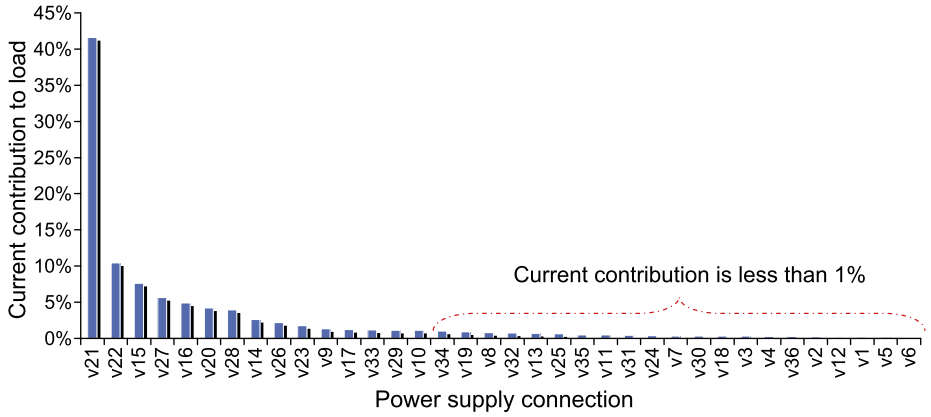

Fig. 13. Percent current provided to the current load L_2 placed within a uniform power grid via the power supply connections, as illustrated in Fig. 11. Note that more than 40% of the current is provided by the closest power supply connection, V_{21}. The current contribution of a supply connection is significantly smaller with distance.

illustrated in Fig. 14. When the grid size is larger than 30×30, the error is less than 0.5% of the supply voltage. Modern power grids can contain more than a million nodes. The size of these grids typically exceed 1000×1000, making the approximation error effectively zero.

A power grid is divided into smaller partitions [11,13] to exploit the principle of spatial locality. Each partition is analyzed individually and a complete solution is obtained by combining the results of each partition. The ideal solution is obtained with only one partition (*i.e.*, no partitioning), thereby considering all of the interactions among each power supply and load circuit. This approach suffers from long computational time. The fastest solution is obtained when the power grid is divided into the smallest possible partitions. This analysis, however, can introduce significant error. A tradeoff in partition size therefore exists between computational complexity and accuracy.

For each partition, the error is smallest in the middle of the partition and increases toward the boundaries. A partitioning approach divides the power grid into several overlapping windows where only the middle of each window is analyzed. The boundaries of each partition overlap with the adjacent partitions. This method of overlapping windows has been shown to be effective in industrial power grids to accelerate the power grid analysis process [11]. Some redundancy is introduced during the analysis process which significantly reduces the error from application of spatial locality. This partitioning approach is illustrated in Fig. 15 where a flip-chip power grid with several C4 connections is partitioned into four overlapping windows. Each window consists of an analysis partition and an overlapping boundary. The size of each partition and overlapping boundary is chosen sufficiently large to minimize the error caused by the partitioning process. A tradeoff therefore also exists between computational complexity and induced error in the size of the overlapping boundary. When the size of the overlapping boundary is sufficiently large, the effect of the adjacent power grid partition is minimized. Alternatively, the computational complexity of the analysis process decreases when the size of the overlapping boundary is small. In this paper, the size of each partition and the overlapping boundary is maintained larger than 100×100 and 20, respectively, making the approximation error less than 0.1%. The partitioning approach also considers the locally uniform, globally non-uniform nature of the power grid. Each partition is treated as a uniform power grid. Different partitions can exhibit different impedance characteristics.

4.4. Error correction windows

Several error reduction techniques can be implemented within this algorithm. One technique is the use of error correction windows, as illustrated in Fig. 16, where the supply connections, load circuits, error correction window, and analysis window are shown, respectively, with a light dot, dark dot, light gray box, and green box. Since the voltage at each supply connection is known

a priori, the induced error at a supply connection is the difference between the ideal supply voltage and the voltage determined from this algorithm. This error is primarily introduced when determining the current contribution of a power supply connected to the power grid. A correlation exists between the error at the supply connection node and the nodes within close proximity of the power supply. The error is generally maximum at the supply connection node and is lower with increasing distance from the supply. An error correction window for each supply is constructed based upon the error at the supply connection node. By introducing this error correction technique, the maximum error is reduced to less than 0.3% of the supply voltage, as described in Section 5.

5. Experimental results

The validity of these algorithms to efficiently analyze a power grid for several scenarios is presented in this section. The algorithms are implemented using MATLAB and the computations are performed on a Unix workstation with a 3 GHz CPU and 10 GB of RAM. The accuracy of Algorithms I, II, and III is compared with SPICE simulations. For simplicity, the resistance between two adjacent nodes in the power grid is assumed to be 1 Ω and the voltage sources are assumed to be 1 V. The current loads are between 1 mA and 100 mA.

The validity of the closed-form expression for one voltage supply and one current load is analyzed with a 1 V supply connected at $N_{3,3}$ and the load sinking 100 mA at $N_{5,4}$. The maximum error is 1.44 mV, less than 0.2% of the voltage at that node, as determined with SPICE. The error of the corresponding node voltages as compared to SPICE is listed in Table 2. The italicized value is the supply node and the bold value is the node connected to the current load.

Nodal voltage analysis of a power grid with one voltage supply and multiple current loads is evaluated when the voltage supply is connected to $N_{4,4}$ and four current loads are arbitrarily placed at

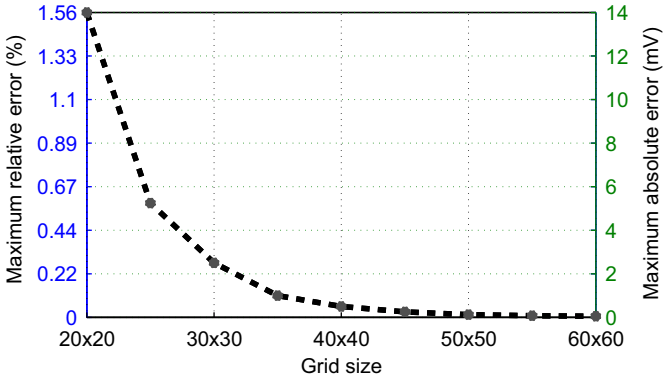

Fig. 14. Maximum error for different grid size assuming a model of a finite power grid with an infinite mesh structure. The percent relative error as compared to SPICE and the absolute error are shown, respectively, on the left and right axes. Note that the error decreases significantly with increasing grid size.

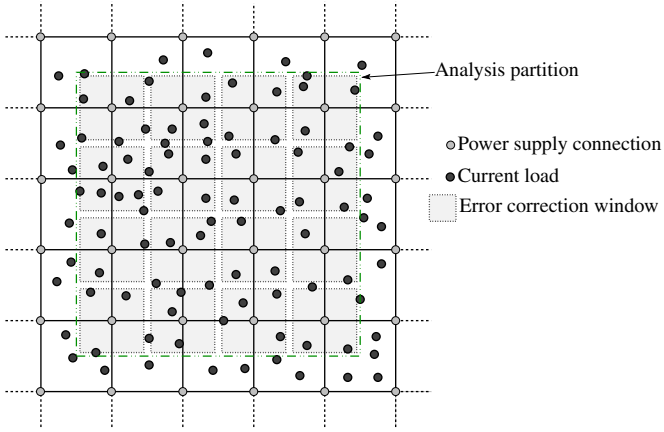

Fig. 16. Partition of a resistive flip-chip power grid with supply connections and load circuits denoted, respectively, with light and dark dots. The error correction windows are shown with small gray boxes around each supply connection node. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

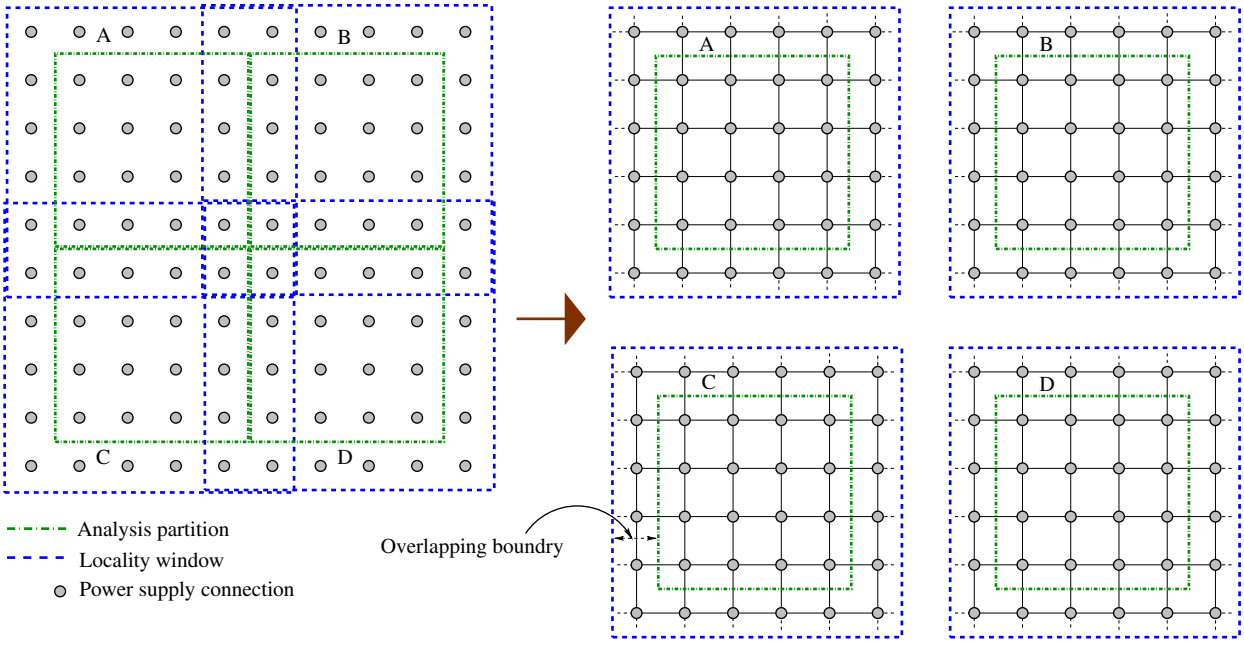

Fig. 15. Power grid divided into smaller partitions. Each partition consists of an analysis partition and overlapping boundary.

$N_{1,7}$, $N_{2,3}$, $N_{6,6}$, and $N_{2,7}$. In this case, each load sinks 25 mA from the power grid. The error of Algorithm II as compared to SPICE is listed in Table 3. The maximum error of the proposed algorithm as compared to SPICE is 1.1 mV (less than 0.2%).

The validity of Algorithm III is analyzed with three voltage supplies and a current load connected arbitrarily to the power grid. The current load sinks 100 mA current and the voltage supplies are 1 V. The maximum voltage drop is less than 100 mV. The error of Algorithm III as compared to SPICE is tabulated in Table 4. The maximum error is 1.41 mV which is smaller than 0.2% of the voltage, as determined with SPICE.

The complete algorithm, Algorithm IV, is validated for a larger power grid with multiple voltage supplies and multiple current loads arbitrarily placed within a 17×17 power grid. The results of Algorithm IV are compared with SPICE and the error is tabulated in Table 5. The current loads sink between 1 mA and 100 mA from the grid and the voltage supplies are 1 V. The maximum error is 4.03 mV which is less than 0.5% of the voltage, as determined with SPICE. When the error correction is applied to Algorithm IV, the maximum error is reduced to 2.35 mV, which is less than 0.3% as compared to SPICE simulations, as tabulated in Table 6. Note that the nodes are shown in italic font if error correction has been applied.

The computational complexity of the random walk technique is $O(LMN)$ [23] where N is the number of nodes without power supply connections, L is the number of steps in a single walk, and M is the number of walks to determine the voltage at a node. The random walk method is faster for flip chip power grids as compared to wire-bonded power grids or power grids with a limited number of on-chip power supplies since M is significantly larger. The computational complexity of the random walk method can, however, be decreased with hierarchical methods [23,24], although the property of locality is sacrificed.

Alternatively, the computational complexity of the proposed method is linear with the size of the power grid. Since no iterations are required (*i.e.*, $L=1$) and the voltage is determined with closed-form expressions (*i.e.*, $M=1$), the computational complexity is $O(N)$. Although converting the voltage sources to equivalent current sources also requires computational effort, this computational procedure is a one time process, and the additional computational complexity is negligible. The computational complexity also does not depend on the type of power grid (*e.g.*, the same computational complexity for flip chip power grids, wire-bonded power grids, and power grids with on-chip power supplies).

To compare the computational runtime of this method with previously proposed techniques, five differently sized circuits with evenly distributed C4 bumps 25 nodes from each other are considered. The runtime of the proposed algorithm is compared with the random walk method in [8] and the second order iterative method in [10], as shown in Table 7. The partition size for all of the circuits when utilizing locality is larger than 100×100 to maintain an approximation error of less than 0.1%. The random walk method is applied for 20,000 iterations on each circuit to accurately determine the node voltages. The number of iterations of the random walk and second order iterative methods is chosen to maintain a maximum error of less than 5 mV as compared to the results with 20,000 iterations. The error of the proposed method is also less than 5 mV for each circuit. This method with locality is over 60 and two times faster as compared to the random walk and second order iterative methods, respectively, for power grids smaller than five million nodes. For circuit sizes greater than 25 million nodes (*e.g.*, Circuits IV and V listed in Table 7), the proposed algorithm with locality is over 175 times and three times faster as compared to the random walk and second order iterative methods, respectively. The runtime of the random walk method depends strongly upon the number of power supply connections. When the number of power supply connections decreases, the computational runtime of the random walk method dramatically increases. Alternatively, the computational runtime of the proposed method is lower with fewer number of power supply connections.

Table 2
Error of Algorithm I as compared to SPICE. The voltage supply is connected at $N_{3,3}$ (italic) and the load device is connected at $N_{5,4}$ (bold). The maximum error is less than 0.2% of the supply voltage.

	1	2	3	4	5	6	7	8
1	−0.12	−0.05	0.46	−0.27	−0.49	−0.26	−0.125	−0.15
2	−0.09	−0.55	0.79	0.152	−0.68	−0.37	−0.554	−0.14
3	0.33	0.62	*0*	1.13	−0.52	0.52	0	−0.26
4	−0.31	−0.83	0.21	−1.44	**−0.31**	−0.93	−0.64	−0.41
5	−0.25	−0.27	0.37	0.24	−1.10	0.24	−0.22	−0.38
6	−0.18	−0.04	0.18	−0.04	−0.77	−0.25	−0.18	−0.30
7	−0.13	−0.01	0	−0.23	−0.50	−0.36	−0.28	−0.30
8	−0.14	−0.04	−0.08	−0.27	−0.32	−0.34	−0.34	−0.34

Table 3
Error of Algorithm II as compared to SPICE. The voltage supply is connected at $N_{4,4}$ (italic) and the load devices are connected at $N_{1,7}$, $N_{2,3}$, $N_{6,6}$, and $N_{7,2}$ (bold). The maximum error is less than 0.2% of the supply voltage.

	1	2	3	4	5	6	7	8
1	−0.17	−0.24	−0.06	0.07	−0.16	−0.38	**−0.19**	−0.30
2	0.01	−0.40	−0.06	0.32	−0.20	−0.14	−0.36	−0.03
3	−0.23	**−0.25**	−0.80	0.60	−0.64	−0.25	−0.18	−0.02
4	0.28	0.11	0.76	*0*	0.69	0.18	0.05	0.02
5	0.01	−0.40	−0.64	0.75	−0.50	−0.42	−0.06	−0.04
6	0	−0.49	−0.08	0.28	−0.39	**−0.31**	−0.36	−0.23
7	−0.40	**−0.25**	−0.32	0.12	−0.04	−0.45	−0.07	−0.13
8	−0.05	−0.35	1.11	0.08	−0.02	−0.29	−0.16	−0.17

Table 4
Error of Algorithm III as compared to SPICE. Power supplies are connected at $N_{1,2}$, $N_{6,8}$, and $N_{8,1}$ (italic) and current load is connected at $N_{5,4}$ (bold). The maximum error is 1.41 mV (less than 0.2% of the the voltage, as determined with SPICE).

	1	2	3	4	5	6	7	8
1	1.33	0.67	0.75	0.62	0.31	0.6	0.71	*0*
2	*1.24*	1.33	1.11	0.87	−0.07	0.54	0.23	0.63
3	1.21	0.49	0.83	1.41	−0.61	1.2	0.45	0.47
4	0.77	0.32	−0.09	−0.58	**0.44**	−0.63	−0.27	0.15
5	0.67	0.62	0.65	1.36	−0.62	1.42	0.62	0.35
6	0.74	0.69	0.7	0.62	−0.3	0.8	0.57	0.41
7	0.65	0.68	0.6	0.4	−0.15	0.78	0.27	0.42
8	0.68	0.7	0.6	0.68	0.71	*0.34*	0.87	0.72

6. Conclusions

Closed-form expressions for fast *IR* voltage drop analysis of large power grids with non-uniform current loads and voltage supplies are proposed in this paper. A closed-form effective resistance model for semi-uniform power grids is described. Four different algorithms for multiple supply voltage and current load placement configurations are presented. Since the proposed algorithms utilize closed-form expressions, the runtime is significantly less than previously proposed power grid analysis methods while exhibiting reasonable error (*i.e.*, less than 4.03 mV for Algorithm IV, an error of less than 0.5% as compared to SPICE). With the introduction of locality and error correction windows, the error decreases to 2.35 mV, which is

Table 5
Error of Algorithm IV as compared to SPICE. Power supplies are connected at the corners (italic) and current loads are connected at various nodes (bold). The maximum error is 4.03 mV (less than 0.5% of the voltage, as determined with SPICE). Error correction is not used in this example and the maximum error occurs at the supply connection.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	*0*	0.36	**0.10**	−0.25	−0.32	−0.43	−0.57	−0.53	−0.28	0.07	0.39	0.87	1.1	1.71	2.26	3.06	*4.03*
2	0.4	−0.52	−0.4	−0.29	−0.45	−0.67	−0.93	−1.15	−0.68	−0.18	0.22	0.65	**1.08**	1.43	1.76	1.87	3.3
3	0.18	−0.27	−0.39	−0.45	−0.58	−0.85	−1.31	**−2.35**	−1	−0.32	0.19	0.62	0.91	1.28	1.56	**1.94**	2.5
4	−0.12	−0.24	−0.36	−0.44	−0.49	−0.73	−1.09	−1.17	−0.64	−0.2	0.24	0.56	0.84	1.22	1.55	1.75	2.1
5	−0.2	−0.26	−0.31	−0.36	−0.42	−0.46	−0.93	−0.56	−0.25	0.01	0.28	0.55	0.89	1.19	1.42	1.65	1.83
6	−0.28	−0.3	−0.38	−0.38	−0.31	−0.07	−0.9	−0.01	−0.07	0.09	0.23	0.58	0.89	1.12	1.37	1.48	1.66
7	−0.33	−0.29	−0.31	−0.44	−0.56	−0.83	**−0.27**	−0.54	−0.17	0.14	0.2	0.69	0.93	1.12	1.25	1.44	1.61
8	−0.34	−0.3	−0.34	−0.22	−0.15	−0.11	−0.28	0.43	0.2	0.57	0.18	0.96	0.91	1.06	1.25	1.43	1.48
9	−0.36	−0.33	−0.35	−0.23	0.18	−0.4	0.03	0.11	−0.16	0.12	**0.59**	0.39	0.67	0.99	1.18	1.35	1.52
10	−0.46	**−0.47**	−0.4	−0.48	−0.54	**−0.2**	−0.46	0.15	−0.06	0.99	0.3	1.05	1	1.15	1.19	1.38	1.51
11	−0.44	−0.48	−0.36	−0.24	0.07	−0.62	0.05	−0.11	**0.37**	0.16	0.21	0.75	1.02	1.25	1.28	1.55	1.56
12	−0.48	−0.5	−0.35	−0.3	−0.14	−0.36	0.17	0.6	0.13	0.81	0.58	0.84	1.05	1.18	1.37	1.44	1.67
13	−0.55	−0.48	−0.48	−0.37	−0.27	−0.18	0.1	0.3	0.26	0.7	0.68	1.02	1.14	1.38	1.39	1.74	1.84
14	−0.6	−0.65	−0.64	−0.53	−0.24	−0.12	0.12	0.2	0.28	0.51	**0.87**	0.97	1.15	**1.37**	1.55	1.8	2.06
15	−0.7	−0.93	−0.77	−0.55	−0.25	−0.09	0.09	0.24	0.44	0.68	0.82	1.09	1.29	1.44	1.66	1.91	2.39
16	−0.95	−1.58	−0.94	**−0.56**	−0.32	**−0.11**	0.03	0.25	0.46	0.72	0.88	1.12	1.35	1.57	1.83	1.89	3.04
17	*−2.49*	−0.84	−0.46	−0.51	−0.16	−0.03	0.16	0.3	0.52	0.65	0.84	1.14	1.37	1.73	2.21	2.92	*3.47*

Table 6
Error of Algorithm IV with error correction windows as compared to SPICE. The nodes where error correction is applied is shown in italic font. The maximum error is 2.35 mV which is less than 0.3% of the voltage, as determined with SPICE. The location of the power supplies and current loads are denoted, respectively, as bold and underine values.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	**0**	0.36	0.1	−0.25	−0.32	−0.43	−0.57	−0.53	−0.28	0.07	*−0.19*	*−0.28*	*−0.63*	*−0.59*	*−0.62*	*−0.39*	***0***
2	0.4	−0.52	−0.4	−0.29	−0.45	−0.67	−0.93	−1.15	−0.68	−0.18	*−0.36*	*−0.5*	*−0.65*	*−0.87*	*−1.12*	*−1.58*	*−0.15*
3	0.18	−0.27	−0.39	−0.45	−0.58	−0.85	−1.31	−2.35	−1	−0.32	*−0.39*	*−0.53*	*−0.82*	*−1.02*	*−1.32*	*−0.94*	*−0.38*
4	−0.12	−0.24	−0.36	−0.44	−0.49	−0.73	−1.09	−1.17	−0.64	−0.2	*−0.34*	*−0.59*	*−0.89*	*−1.08*	*−0.75*	*−0.55*	*−0.2*
5	−0.2	−0.26	−0.31	−0.36	−0.42	−0.46	−0.93	−0.56	−0.25	0.01	*−0.3*	*−0.6*	*−0.84*	*−0.54*	*−0.31*	*−0.08*	*0.1*
6	−0.28	−0.3	−0.38	−0.38	−0.31	−0.07	−0.9	−0.01	−0.07	0.09	*−0.35*	*−0.57*	*−0.26*	*−0.03*	*0.22*	*0.33*	*0.51*
7	−0.33	−0.29	−0.31	−0.44	−0.56	−0.83	−0.27	−0.54	−0.17	0.14	*−0.38*	*0.11*	*0.35*	*0.54*	*0.67*	*0.86*	*1.03*
8	−0.34	−0.3	−0.34	0.22	−0.15	−0.11	−0.28	0.43	0.2	0.57	0.18	0.96	0.91	1.06	1.25	1.43	1.48
9	−0.36	−0.33	−0.35	−0.23	0.18	−0.4	0.03	0.11	−0.16	0.12	0.59	0.39	0.67	0.99	1.18	1.35	1.52
10	−0.46	−0.47	−0.4	−0.48	−0.54	−0.2	−0.46	0.15	−0.06	0.99	0.3	1.05	1	1.15	1.19	1.38	1.51
11	*−0.08*	*−0.12*	*0*	*0.12*	*0.43*	*−0.26*	*0.41*	−0.11	0.37	0.16	*−0.29*	*0.25*	*0.52*	*0.75*	*0.78*	*1.05*	*1.06*
12	*0.23*	*0.21*	*0.36*	*0.41*	*0.57*	*0.35*	*0.53*	0.6	0.13	0.81	*0.08*	*−0.15*	*0.06*	*0.19*	*0.38*	*0.45*	*0.68*
13	*0.52*	*0.59*	*0.59*	*0.7*	*0.8*	*0.53*	*0.46*	0.3	0.26	0.7	*0.18*	*0.03*	*−0.35*	*−0.11*	*−0.1*	*0.25*	*0.35*
14	*0.82*	*0.77*	*0.78*	*0.89*	*0.83*	*0.59*	*0.48*	0.2	0.28	0.51	*0.37*	*−0.02*	*−0.34*	*−0.61*	*−0.43*	*−0.18*	*0.08*
15	*1.08*	*0.85*	*1.01*	*0.87*	*0.82*	*0.62*	*0.45*	0.24	0.44	0.68	*0.32*	*0.1*	*−0.2*	*−0.54*	*−0.82*	*−0.57*	*−0.09*
16	*1.18*	*0.55*	*0.84*	*0.86*	*0.75*	*0.6*	*0.39*	0.25	0.46	0.72	*0.38*	*0.13*	*−0.14*	*−0.41*	*−0.65*	*−1.08*	*0.07*
17	*0*	*1.29*	*1.32*	*0.91*	*0.91*	*0.68*	*0.52*	0.3	0.52	0.65	*0.34*	*0.15*	*−0.12*	*−0.25*	*−0.27*	*−0.05*	***0***

Table 7
Runtime comparison.

	#nodes	Random walk [8](min:sec)	Second order iterative [10](min:sec)	Proposed algorithm	
				No partitioning (min:sec)	Locality and error correction (min:sec)
Circuit I	250 K	4:22	0:03	0:10	0:03
Circuit II	1 M	15:08	0:47	0:32	0:13
Circuit III	4 M	59:46	1:33	2:19	0:58
Circuit IV	25 M	1156:14	19:49	17:13	6:33
Circuit V	49 M	3418:05	46:38	38:55	13:09

less than 0.3% of the voltage, as determined with SPICE. Previously proposed *IR* drop analysis methods iteratively solve the power grid to determine the node voltages. These methods require the voltage at all of the nodes adjacent to the analysis node to be determined. Determining the voltage at a particular node therefore requires the computation of the voltage at nearby nodes which may not be of interest. Alternatively, the proposed algorithms presented in this paper can compute the voltage at any particular node in a power grid without determining the voltage at the adjacent nodes. The proposed algorithm can therefore be applied to localized power grid analysis.

Appendix A. Effective resistance model

To determine the effective resistance between nodes n_{x_1,y_1} and n_{x_2,y_2}, the principal of superposition is applied in two steps. First,

the current I is introduced at n_{x_1,y_1} and exits the grid at the boundaries (*i.e.*, at infinity). The current from n_{x_1,y_1} to the adjacent nodes is determined by the resistance between n_{x_1,y_1} and the adjacent nodes. Secondly, current I is introduced at infinity and exits the power grid at n_{x_2,y_2}. The current from the adjacent nodes to n_{x_2,y_2} is found similarly. By applying superposition in these two steps, the current I is modeled as entering the power grid from n_{x_1,y_1} and exiting the grid at n_{x_2,y_2}. The effective resistance between n_{x_1,y_1} and n_{x_2,y_2} can therefore be written as $R_{eff} = 2(V_{x_1,y_1} - V_{x_2,y_2})/I$ [16,25].

When a current source is connected to $n_{x,y}$, this current can be described in terms of the adjacent node voltages and corresponding resistances as

$$I_{x,y} = \frac{(2k+2)V_{x,y} - (kV_{x,y+1} + kV_{x,y-1} + V_{x+1,y} + V_{x-1,y})}{kr}. \tag{A.1}$$

Applying separation of variables, substituting $V_{x,y} = e^{x\alpha + jy\beta}$ where $k+1 = k\cos\beta + \cosh\alpha$, and after some simplifications, the current at $n_{0,0}$ can be written as

$$i_{0,0} = \frac{(2k+2)V_{0,0} - kV_{0,1} - kV_{0,-1} - V_{1,0} - V_{-1,0}}{kr}. \tag{A.2}$$

Applying certain trigonometric identities and Euler's formula, $i_{0,0}$ is

$$i_{0,0} = 2\sinh\alpha/kr. \tag{A.3}$$

Similarly, the current at $n_{0,y}$ is

$$i_{0,y} = 2\sinh\alpha\cos y\beta/kr. \tag{A.4}$$

The voltage at an arbitrary node $n_{x,y}$ is the sum of all β values

$$V_{x,y} = \int_0^{\pi} F(\beta) v_{x,y}(\beta)\, d\beta, \tag{A.5}$$

where $F(\beta)$ is a function that satisfies a current source at $n_{0,0}$, and no current source exists at $n_{0,y}$ when $y \neq 0$. Thus, all of the current sources other than at $n_{0,0}$ are effectively eliminated [16]. The corresponding current at $n_{x,y}$ is

$$I_{x,y} = \int_0^{\pi} F(\beta) i_{x,y}(\beta)\, d\beta. \tag{A.6}$$

From inspection, $F(\beta)$ is

$$F(\beta) = \frac{kIr}{2\pi\sinh\alpha}, \tag{A.7}$$

to satisfy (A.5) when only one current source located at $n_{0,0}$ is present within the power grid. Substituting (A.7) into (A.5), the voltage at $n_{x,y}$ is

$$V_{x,y} = \frac{kIr}{2\pi}\int_0^{\pi} \frac{e^{-|x|\alpha}\cos y\beta}{\sinh\alpha}\, d\beta. \tag{A.8}$$

Substituting (A.8) into $R_{eff} = 2(V_{x_1,y_1} - V_{x_2,y_2})/I$, the effective resistance between $n_{0,0}$ and $n_{x,y}$ is

$$R_{x,y} = \frac{k\,r}{\pi}\int_0^{\pi} \frac{(2 - e^{-|x|\alpha}\cos y\beta)}{\sinh\alpha}\, d\beta. \tag{A.9}$$

$R_{x,y}$ is solved by dividing the integral into two, and writing (A.9) as a sum of two integrals, $R_{x,y}/r = R_{1(x,y)} + R_{2(x,y)}$

$$R_{x,y}/r = \frac{\sqrt{k}}{\pi}\int_0^{\pi} \frac{(1 - e^{-x\sqrt{k}|\beta|}\cos n\beta)}{\beta}\, d\beta + \frac{k}{\pi}\int_0^{\pi}\left[\frac{1}{\sqrt{(k+1-k\cos\beta)^2 - 1}} - \frac{1}{\beta\sqrt{k}}\right] d\beta. \tag{A.10}$$

The first integral $R_{1(x,y)}$ is solved using an exponential integral [16,26]

$$R_{1(x,y)} = \frac{\sqrt{k}}{2\pi}[\ln(x^2 + ky^2) + 2(0.57721 + \ln\pi)], \tag{A.11}$$

while the second integral $R_{2(x,y)}$ is solved numerically, assuming k approaches 1

$$R_{2(x,y)} = -0.033425k - \frac{k(k-1)0.1975}{\pi}. \tag{A.12}$$

The effective resistance between two arbitrary nodes $R_{x,y}$ is therefore

$$R_{x,y}/r = \frac{\sqrt{k}}{2\pi}[\ln(x^2 + ky^2) + 3.44388] - 0.033425\,k - \frac{k(k-1)0.1975}{\pi}. \tag{A.13}$$

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