Shielding Methodologies in the Presence of Power/Ground Noise

Selçuk Köse, Emre Salman, *Student Member, IEEE*, and Eby G. Friedman, *Fellow, IEEE*

***Abstract*—Design guidelines for shielding in the presence of power/ground (P/G) noise are presented in this paper. The effect of P/G noise on crosstalk is analyzed for different line lengths, line widths, and interconnect driver resistances. Considering the P/G noise, a shield line can *degrade* rather than enhance signal integrity due to increased P/G noise coupling on the victim line. A 2π *RLC* interconnect model is used to investigate the effects of both coupling capacitance and mutual inductance on the crosstalk noise. Physical spacing and shield insertion are compared in terms of the coupling noise on the victim line for several technology nodes. Boundary conditions are also provided to determine the effective range of spacing and shield insertion in the presence of P/G noise. Additionally, the effects of technology scaling on P/G noise and shielding efficiency are discussed, and related design tradeoffs are addressed.**

***Index Terms*—Coupling capacitance, crosstalk noise, crosstalk reduction techniques, dI/dt noise, interconnect, mutual inductance, power/ground (P/G) noise, shield insertion, spacing.**

I. Introduction

In DEEP submicrometer integrated circuits, crosstalk between adjacent interconnect lines has become a primary design issue. With aggressive technology scaling, the local interconnect has become more resistive and capacitive. The global interconnect has become more inductive. Capacitive and inductive coupling has therefore become a significant design issue in global interconnect [1]–[3].

Shielding is widely used in integrated circuits to mitigate crosstalk between coupled lines. Two types of shielding methods have been developed, passive shielding [1], [2], [4]–[8], and active shielding [9]–[11]. In passive shielding, the power/ground (P/G) lines are routed as shield lines between critical interconnect to minimize the noise coupled from an aggressor to a victim line. Alternatively, active shielding [9]–[11] uses dedicated shield lines with switching signals rather than P/G lines. Although the performance of active shielding in reducing crosstalk noise voltage is superior to passive shielding, active shielding requires additional area and consumes more power.

P/G networks are routed as shield lines in passive shielding to mitigate coupling noise. These P/G shield lines themselves can, however, be noisy. This noise, typically neglected in existing shielding methodologies, is due to inductive dI/dt noise and resistive IR voltage drops. With increasing device densities, the P/G noise voltage can be more than 20% of the supply voltage [12]–[14]. Since the distance between the shield and victim lines is smaller than the distance between the aggressor and victim lines, the P/G noise on the shield line can produce more noise on the victim line than the crosstalk noise coupled from the aggressor to the victim. Hence, while a shield line reduces noise coupling from the aggressor interconnect, the shield line can also *increase* noise coupling due to P/G noise.

Although P/G noise has received significant attention in the design of robust power distribution networks [12]–[15], existing works do not consider the deleterious effects of P/G noise on *shielding methodologies* [1], [2], [4]–[7], [9]–[11], [16]. P/G lines routed as shield lines have typically been treated as *ideal* ground or supply voltage connections, which do not accurately model the effect of noise on the shield line. Recently, noise on the P/G lines is mentioned in [8] without describing the effect of this noise on the victim line and related shielding methodologies. P/G noise on the shield lines is considered in this paper to provide practical and more effective shielding methodologies.

An alternative method to reduce crosstalk is to increase the distance between the aggressor and victim lines without inserting a shield line. Tradeoffs between the two methods, shield insertion and physical spacing, are discussed in [4] and [5] without considering P/G noise on the shield lines. P/G noise, however, can significantly affect the decision criteria between shielding and spacing, as discussed throughout this paper. The primary objective of this paper is to investigate the effect of P/G noise on shield lines within a passive shielding methodology. Comparisons between physical spacing and shield insertion techniques are provided. Boundary conditions are also identified to determine the efficacy regions of spacing and shield insertion. Once P/G noise is considered, spacing alone can be more useful than shield insertion under specific conditions, as described in this paper. These results provide decision criteria in choosing between spacing or shielding in a noisy environment.

This paper is organized as follows. Background material is provided in Section II. In Section III, the effects of several technology and design parameters characterizing the interconnect and shield lines in terms of crosstalk noise on the victim line are investigated. Finally, this paper is concluded in Section V.

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II. Background

Background material is provided in this section for evaluating the effect of P/G noise on passive shielding methodologies. Specifically, an overview of crosstalk reduction techniques is provided in Section II-A. An interconnect model and the design criterion used throughout this paper are introduced in Section II-B. The P/G noise model and the effect of this noise on crosstalk noise are described in Section II-C.

A. Crosstalk Noise Reduction Techniques

Several techniques can be used to mitigate the effects of crosstalk noise in high complexity integrated circuits [1]–[7], [9]–[11], [16]. A brief overview of these techniques is provided in this section.

Increasing the physical distance between the aggressor and victim lines can reduce the coupling capacitance and mutual inductance between adjacent lines. The reduction in crosstalk capacitance is approximately inversely proportional with the increase in spacing. The mutual inductance, however, is not significantly reduced with increasing distance since the mutual inductance is a long range phenomenon. To reduce the mutual inductance, additional return paths should be provided for the current to flow.

Inserting shield lines between the aggressor and victim lines reduces the capacitive and inductive coupling between adjacent blocks [1], [2], [4]–[7]. Shield insertion significantly reduces capacitive coupling between the aggressor and victim lines because capacitive coupling is a short range phenomenon and is significantly reduced in nonadjacent lines. Shield insertion moderately reduces the mutual inductance due to the current return path formed by the inserted shield line for both the aggressor and victim lines [7]. The difficulty in forcing the current return path complicates the inductive shielding process.

Active shielding is another shielding technique in which the shield line switches depending upon the switching pattern of the adjacent bus lines [9]–[11]. Capacitive (inductive) coupling is reduced with active shielding when the shield line is switched in the same (opposite) direction as the signal line [10]. The switching activity of the shield lines should therefore be tuned to the switching pattern which is different for RC dominated and LC dominated interconnect lines. The primary drawback of active shielding is increased power consumption and additional area of the logic circuitry controlling the active shield lines. Furthermore, process and environmental variations may unexpectedly affect the signal arrival times, degrading the efficiency of active shielding.

Sizing the buffer driving the aggressor and victim lines is another technique to reduce crosstalk noise, [6]. The effective conductance of the driver increases with larger drivers. For the victim line, a larger driver can be used to maintain the victim line at a constant voltage by increasing the driver conductance. For the aggressor line, using a smaller driver decreases the crosstalk noise since the signal transition is slower due to the increased RC time constant, decreasing the induced noise on the victim line [6]. Proper sizing of the driver on the aggressor and victim lines can therefore produce lower crosstalk noise. This technique is however subject to delay constraints since a smaller driver increases the gate delay. Wire sizing can also be used to modify the line resistance, coupling capacitance, line-to-substrate capacitance, and self-inductance [17].

Repeater insertion is used to reduce the length of the long interconnect to decrease the line resistance and the coupling capacitance and mutual inductance between lines [18]. Since the length of the switching portions of the adjacent lines decreases with additional inserted repeaters, the crosstalk noise on the victim line is reduced. The switching portions of the adjacent lines can be further reduced by interleaving repeaters [19]. Repeaters, however, consume power and area. Additionally, the jitter induced from each repeater can degrade the performance of certain sensitive signals such as the clock. The primary focus of this paper is to investigate passive shielding methodologies in the presence of P/G noise. Design guidelines are provided for choosing between spacing and shield insertion to enhance signal integrity under different conditions, as described in the following sections.

B. Coupled Interconnect Model and Decision Criterion

A typical interconnect model with a shield line inserted between the aggressor and victim lines is depicted in Fig. 1(a), [4], [5]. The noise on the shield line is modeled as a single voltage source at the near end. The interconnect model used for physical spacing is depicted in Fig. 1(b).

The objective is to compare the effect of inserting a shield line and physical spacing on the coupling noise at the far end of a victim line (sense node). The ratio K of the total coupling noise at the sense node when only a shield line is present, $V_{\text{sense\_with\_shielding}}$, to the total coupling noise when only physical spacing is used, $V_{\text{sense\_with\_spacing}}$, is the decision criterion used to determine the boundary conditions

$$K = \frac{V_{\text{sense\_with\_shielding}}}{V_{\text{sense\_with\_spacing}}}. \tag{1}$$

If $K < 1$, inserting a shield line between the aggressor and victim lines is preferable because the crosstalk noise at the sense node is smaller with a shield than with additional spacing. Alternatively, if $K > 1$, increasing the spacing is a more effective technique. $K = 1$ is therefore treated as a design threshold. Spacing is more efficient above the threshold while shield insertion is more efficient below the threshold. Note that the area is maintained the same for both shield insertion and physical spacing to provide a fair comparison. The distance between the aggressor and victim lines is the same for both shield insertion and physical spacing, as depicted in Fig. 1. For instance, when the width of the shield line increases by Δw, the distance between the aggressor and victim lines increases by $\Delta\text{w}/2$ to maintain unaltered the distance between the shield line and the aggressor and victim lines. When comparing the effectiveness of shield insertion with physical spacing for a specific example, the distance between the aggressor and victim lines is increased by Δw to satisfy the same area constraints for both the shielding and spacing methods. Alternatively, when the distance between the aggressor and victim lines is increased using the spacing method, the distance between the shield line and the aggressor and victim lines is also increased with the shield insertion method to maintain the same area constraints.

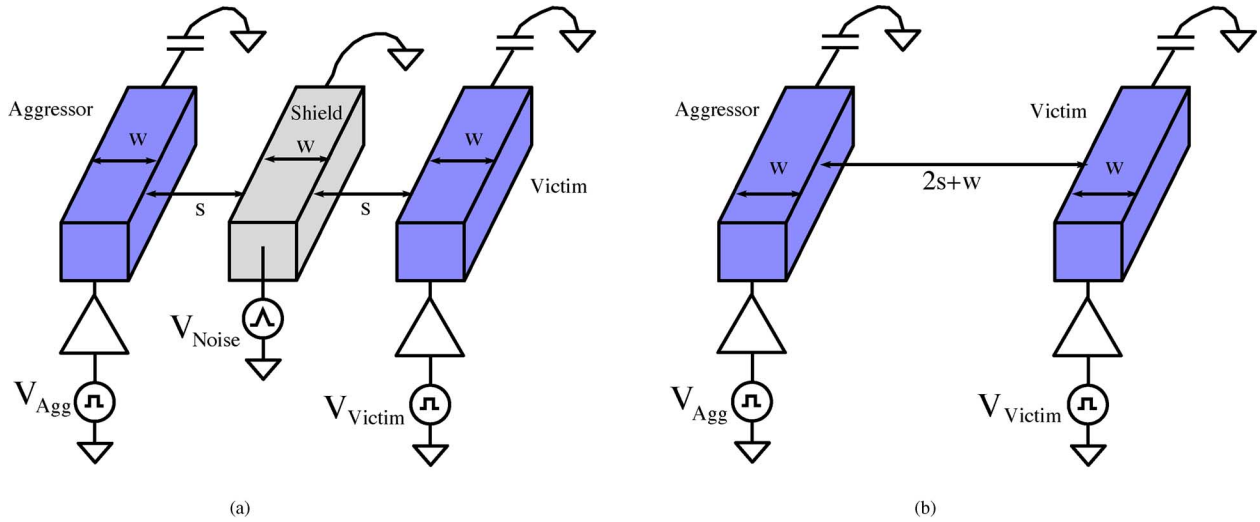

Fig. 1. Global interconnect model for (a) shield line between an aggressor and victim line and (b) physical spacing between an aggressor and victim line. The aggressor and victim lines are modeled with a driver resistance at the near end and terminated with a load capacitance at the far end. P/G noise is modeled as a single voltage source at the near end of the shield line.

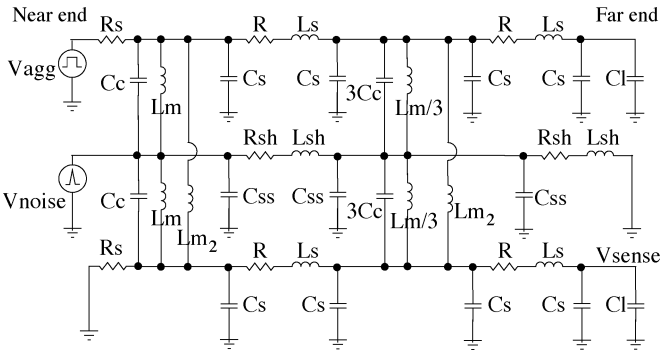

Fig. 2. 2π RLC interconnect model with coupling capacitances and mutual inductances.

To accurately investigate the effects of inductive and capacitive coupling, the 2π RLC interconnect model [4] shown in Fig. 2 is used. The aggressor and victim line parameters, R_s, R, C_s, C_c, C_l, and L_s, represent the interconnect driver resistance, line resistance, line-to-substrate capacitance, coupling capacitance, load capacitance, and self-inductance, respectively. Additional parameters, R_{sh}, L_{sh}, C_{ss}, L_m, and L_{m2}, represent the shield resistance, shield self-inductance, shield line-to-substrate capacitance, mutual inductance between the shield line and the aggressor and victim lines, and mutual inductance between the aggressor and victim lines, respectively. These circuit parameters have been extracted using the IBM Electromagnetic Field Solver Suite Tools (EIP) [20] for the 32-, 45-, and 65-nm technology nodes [21]–[24] for the parameters tabulated in Table I. The operating frequency is 1 Ghz with 100 ps rise and fall transition times. The supply voltage is 1, 0.95, and 0.9 V for the 65-, 45-, and 32-nm technology nodes, respectively.

C. Power/Ground Noise Model

P/G noise has become an important issue in the design of power distribution networks with technology scaling [12]–[14], [25], [26]. The effect of P/G noise on the uncertainty of the data signal delay, clock jitter, noise margin, and gate oxide reliability

TABLE I
INTERCONNECT PARAMETERS FOR 65- [21], 45- [23], AND 32-nm [24] TECHNOLOGY NODES

	W (μm)	S (μm)	T (μm)	H (μm)	ρ (10^{-8}) Ωm
65 nm	0.45	0.45	1.2	0.2	2.2
45 nm	0.40	0.40	0.72	0.2	2.2
32 nm	0.30	0.30	0.504	0.2	2.2

has been well studied [26]. The effect of noise coupling from the power and ground lines used for shielding on the sensitive data and clock lines, however, has not received significant attention. In this section, the detrimental effects of P/G noise on the shield insertion method are discussed.

To exemplify these detrimental effects of P/G noise on shield insertion, a representative noisy ground network is considered, as illustrated in Fig. 3. The power and ground networks are modeled as an inductive-resistive (RL) mesh structure. The active devices are modeled as current sources and the corresponding current profile is modeled as a triangular waveform. Multiple ground connections and active devices are used to more accurately model the ground distribution network. 65-nm technology parameters are assumed.

Due to the resistive and inductive nature of the P/G distribution networks, IR and $L\,dI/dt$ voltage drops degrade the signal integrity. The noise at a particular node strongly depends upon the distance among that node and the location of the ground connections and active devices. The maximum noise of the ground distribution network is maintained below 10% of the supply voltage (i.e., the maximum ground noise is less than 100 mV since, in this case, $V_{\rm DD}$ is 1 V). An arbitrary ground line is used as a shield. The crosstalk noise at the sense node is analyzed assuming a noisy and noise free shield line. The crosstalk noise is approximately five times larger when the shield line is noisy as compared to a noise free shield line, as illustrated in Fig. 4. Note that the detrimental effects of P/G noise are significant for a system even when the ground noise is less than 10% of the supply voltage. With continuous scaling of the supply voltage with each technology generation, the relative magnitude of the

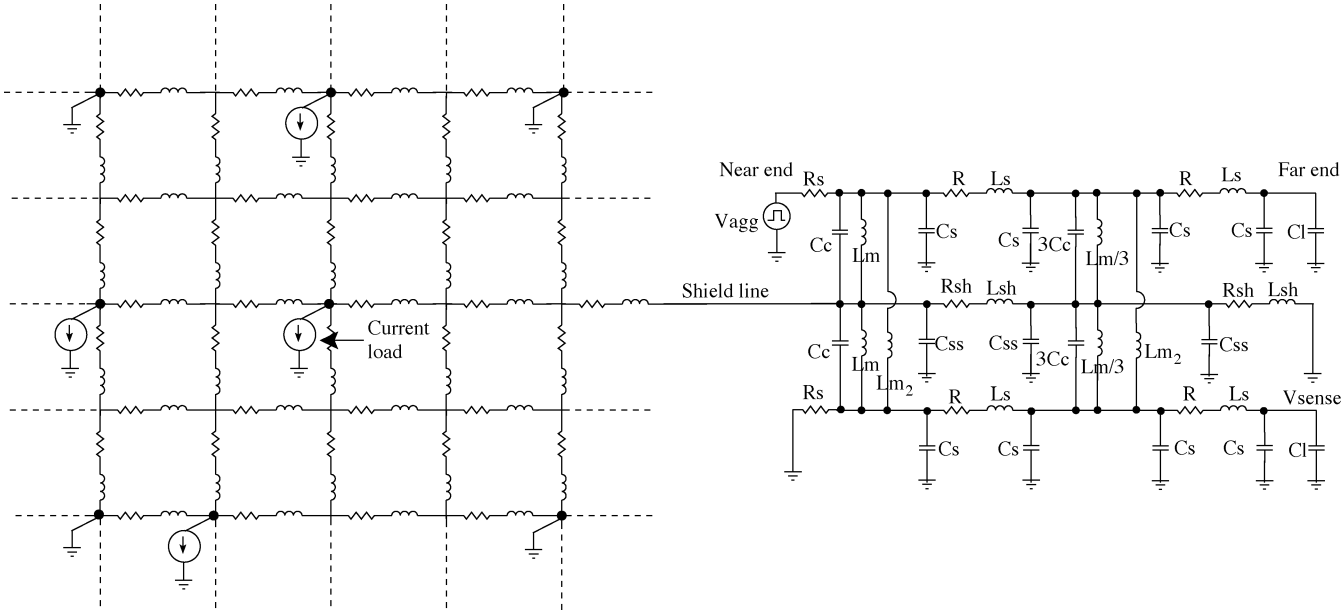

Fig. 3. Ground distribution network used as shield lines to evaluate the effects of P/G noise on the crosstalk noise at the sense node for passive shielding. The ground distribution network consists of multiple ground connections and the current loads are modeled as active devices connected to the ground network.

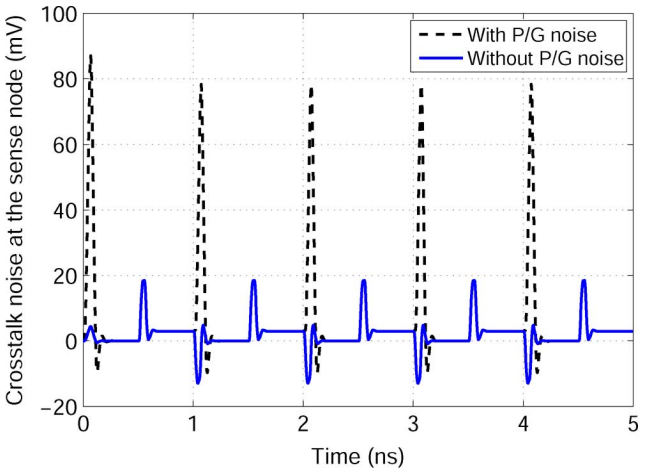

Fig. 4. Crosstalk noise at the sense node with a noisy shield line and a noise free shield line. Note that the crosstalk noise increases dramatically when P/G noise is present on the shield line.

P/G noise to the supply voltage makes the victim lines increasingly sensitive to noise on the shield line.

III. Effects of Technology and Design Parameters on the Crosstalk Noise Voltage

Interconnect capacitance, inductance, and resistance increase with the length of the interconnect. The substrate and coupling capacitances increase and the self-inductance slightly decreases for wider interconnect. The coupling capacitance increases and the self-inductance slightly decreases for thicker interconnects. When the distance between adjacent interconnects increases, the coupling capacitance and mutual inductance decrease and the substrate capacitance increases. These trends are listed in Table II.

The effects of technology scaling on the crosstalk noise voltage and the shield insertion process are discussed in Section III-A. The effects of the interconnect line length and shield line width on the crosstalk noise are discussed in Sections III-B and III-C, respectively. In Section III-D, the effects of the ratio of the interconnect line resistance R_{line} to the interconnect driver resistance R_s on the coupling noise voltage are explored. The effect of the ratio of the line-to-substrate capacitance C_s to the coupling capacitance C_c on the coupling noise is discussed in Section III-E. The effect of the interconnect self- and mutual inductance on crosstalk noise is reviewed in Section III-F.

TABLE II
Effect of Technology and Design Parameters on the Resistance, Capacitance, and Inductance of the Interconnect. Double arrows Illustrate a Significant Change, Single Arrows Illustrate a Minor Change, and $\sim$ Illustrates No Change

	$L \Uparrow$	$W \Uparrow$	$S \Uparrow$	$T \Uparrow$
R	$\Uparrow$	$\Downarrow$	$\sim$	$\Downarrow$
C_s	$\Uparrow$	$\Uparrow$	$\Uparrow$	$\uparrow$
C_c	$\Uparrow$	$\Uparrow$	$\Downarrow$	$\Uparrow$
L_s	$\Uparrow$	$\Downarrow$	$\sim$	$\Downarrow$
L_m	$\Uparrow$	$\sim$	$\Downarrow$	$\sim$

A. Effect of Technology Scaling on the Crosstalk Noise Voltage

The interconnect line parameters change with each technology generation, as listed in Table I. In more advanced technologies, the interconnect is more resistive and the coupling between neighboring lines increases due to higher interconnect densities. A threefold challenge with technology scaling exists in terms of reducing crosstalk noise using shield insertion. First, the P/G network becomes more resistive due to interconnect scaling, increasing the IR voltage drop. The larger IR voltage drop increases the P/G noise on the shield line. Second, supply voltages scale with technology. P/G noise, however, does not scale significantly with technology, increasing the effects of P/G noise on circuit performance. Last, since the distance between adjacent interconnects also scales, the coupling capacitance and mutual inductance between the interconnect lines increase.

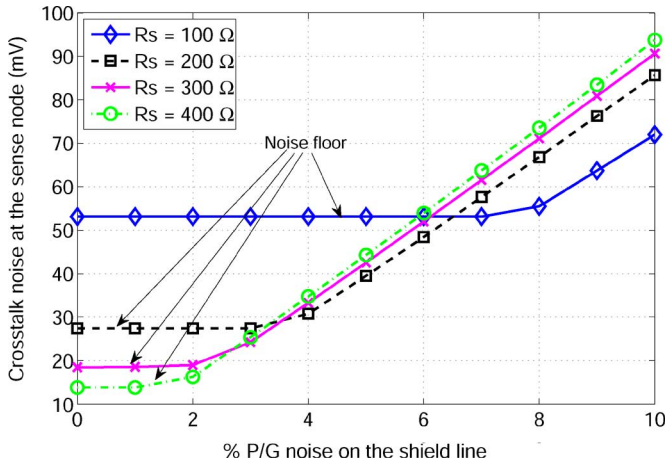

Fig. 5. Crosstalk noise at the sense node as the P/G noise is varied from 0% to 10% of the supply voltage for different driver resistances. Note that a noise floor exist for each driver resistance. This noise floor is due to the noise coupled from the aggressor line to the victim line when P/G noise is less than 7% of the supply voltage with a small driver (i.e., driver resistance is 400 Ω) and less than 2% with a large driver (i.e., driver resistance is 100 Ω).

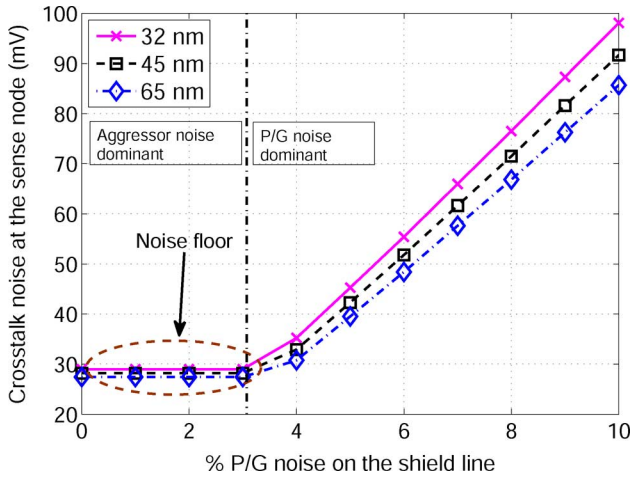

Fig. 6. Crosstalk noise at the sense node for several technology nodes when the P/G noise is varied from 0% to 10% of the supply voltage. The effect of P/G noise on the crosstalk noise increases with each technology generation. The noise floor is due to noise coupling from the aggressor to the victim. P/G noise is dominant when the P/G noise is greater than 3% of the supply voltage. Alternatively, noise coupled from the aggressor is dominant when the P/G noise is less than 3% of the supply voltage.

The crosstalk noise voltage is analyzed for different driver resistances, as illustrated in Fig. 5. When the P/G noise on the shield line is below 2% to 7% of the supply voltage, a higher driver resistance is preferable to minimize the coupling noise at the sense node. When the P/G noise is greater than 2% to 7% of the supply voltage, a lower driver resistance is preferable to minimize the crosstalk noise. Alternatively, when the P/G noise is greater than 7% of the supply voltage, P/G noise is dominant whereas when the P/G noise is lower than 2% of the supply voltage, the dominant noise source is the noise coupled from the aggressor line.

The effect of the magnitude of the P/G noise on the crosstalk noise for different technology nodes is illustrated in Fig. 6. As expected, crosstalk noise is greater in more advanced technologies. Note that the noise floor when the P/G noise is below 3% of the supply voltage is due to the noise coupled from the aggressor.

B. Effect of Line Length on Crosstalk Noise

The length of the global interconnect typically increases with technology scaling, causing greater signal noise [16], [18], [27]. The global interconnect can be longer than 4 mm [16], [18], [27]. Repeater insertion minimizes the crosstalk noise and delay of the long interconnect. Inserting repeaters along the wide and thick global interconnects, however, can cause wire and via congestion as well as dissipate high power [18]. The wire resistance, substrate capacitance, self-inductance of a wire, coupling capacitance, and mutual inductance between neighboring wires increase with longer line length.

For the interconnect model shown in Fig. 2, the coupling noise voltage at the sense node is compared to shield insertion and physical spacing for different interconnect lengths and driver resistances. These results are illustrated in Fig. 7, where $K = 1$ is the threshold (the same noise at the sense node occurs for both physical spacing and shield insertion).

At the 65-nm technology node, the peak value of K occurs at an interconnect length of 1.4 mm. K monotonically increases

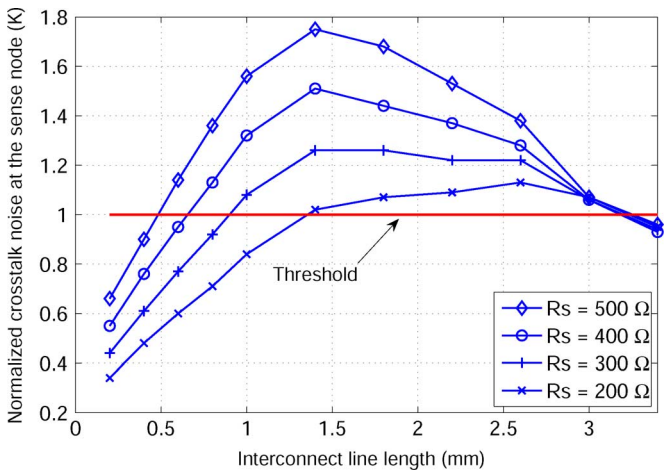

Fig. 7. Effect of interconnect length on crosstalk noise at the sense node for several driver sizes.

for interconnect lines shorter than 1.4 mm and monotonically decreases for interconnect lines longer than 1.4 mm. The crosstalk noise occurring at the sense node with physical spacing and shield insertion is shown in Fig. 8(a) and (b), respectively. The crosstalk noise at the sense node with physical spacing monotonically decreases with longer interconnect length. The crosstalk noise with shield insertion, however, exhibits a non-monotonic behavior since for a short interconnect line, the coupling capacitance and mutual inductance between adjacent lines dominate the line resistance. The crosstalk noise at the sense node, as shown in Fig. 8(b), begins to decrease once the distance between the near and far end of the interconnect line is longer than the length where the effect of the line resistance dominates the effect of the coupling capacitance and mutual inductance (i.e., 1.4 mm for a 65-nm technology). Also note in Fig. 8 that inserting a shield line mitigates the effect of the driver resistance on the crosstalk noise, as discussed in Section III-D. As a result, shield insertion is preferable for shorter lines and spacing is preferable for longer lines.

TABLE III
CRITICAL LINE LENGTH AND DRIVER RESISTANCE FOR SEVERAL ADVANCED TECHNOLOGY NODES. BELOW THE CRITICAL LINE LENGTH, SHIELD INSERTION IS PREFERABLE. PHYSICAL SPACING IS PREFERABLE FOR THOSE INTERCONNECT LINES LONGER THAN THE CRITICAL LINE LENGTH

	65 nm				45 nm				32 nm			
Driver resistance (ohm)	100	200	300	400	100	200	300	400	100	200	300	400
Critical line length (mm)	1.4	1.3	1	0.8	1.3	1.1	0.9	0.8	1.3	0.8	0.2	0.1

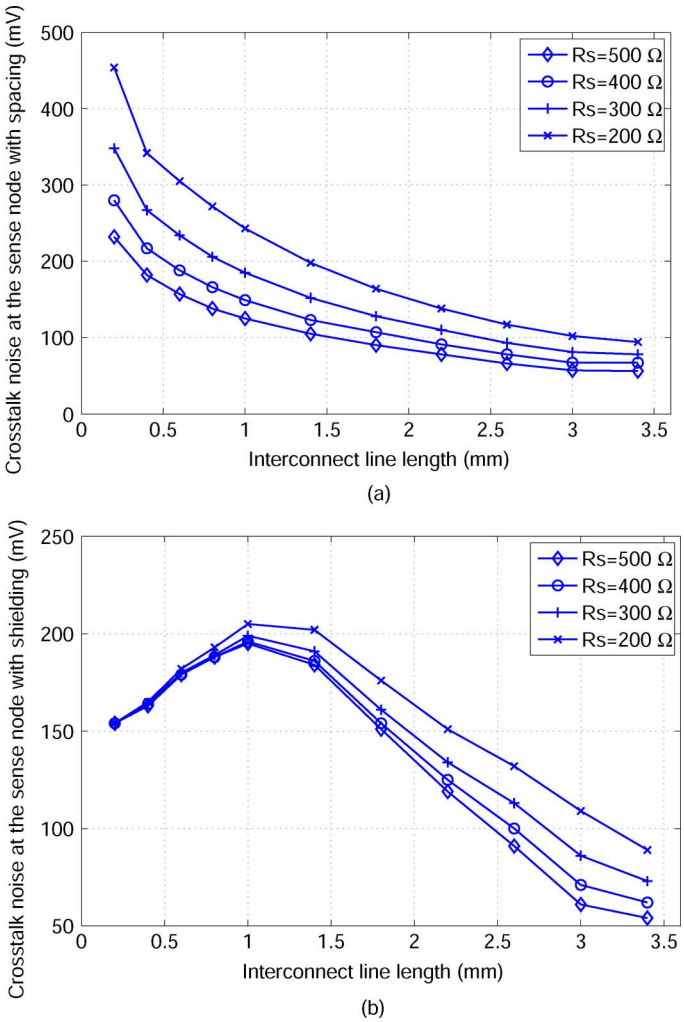

Fig. 8. Crosstalk noise occurring at the sense node for (a) physical spacing and (b) shield insertion. Note that the behavior of the crosstalk noise with shield insertion is non-monotonic with increasing length.

The effect of interconnect length is considered for different technology nodes. The critical interconnect length is determined for different driver resistances, as tabulated in Table III. With each technology generation, the width and thickness of the interconnect scale with the minimum feature size. Since the line resistance increases with each technology generation, larger drivers (e.g., drivers with lower resistance) should be used to drive long victim lines. As listed in Table III, shield insertion is more effective when both the aggressor and victim lines are driven by a large driver.

C. Effect of Shield Line Width on Crosstalk Noise

The effect of the cross-sectional area of the shield line on the coupling noise is discussed in this subsection. As the lines become more narrow and thin, the line resistance increases and the self-inductance decreases, making the lines more resistive.

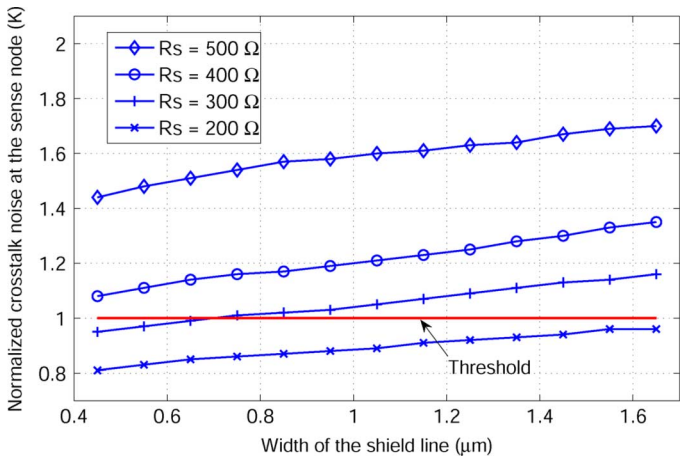

Fig. 9. Effect of shield line width on crosstalk noise for a 1 mm interconnect line. Note that signal integrity with shield insertion is degraded above the threshold line.

The coupling capacitance and mutual inductance between the shield line and the adjacent interconnect do not change significantly. To determine the effect of the cross-sectional area of the shield line on the crosstalk noise, the width of the shield line is evaluated for several driver resistances and interconnect lengths. A comparison of shield insertion and physical spacing is illustrated in Fig. 9 for a 1 mm long interconnect. Note that the distance between the aggressor and victim lines remains the same for both the physical spacing and shield insertion methods.

As the shield line width increases, shield insertion becomes less effective. Although increasing the width lowers the coupling from the aggressor to the sense node, P/G noise coupling to the sense node increases due to the lower resistance of the shield line and the higher mutual inductance. The P/G noise on the shield line propagates from the near end to the far end with less attenuation.

D. Effect of R_{line}/R_s on Crosstalk Noise

The driver resistance has a substantial effect on the behavior of global interconnects [28]–[30]. The driver resistance is less affected with technology scaling [31] because the oxide capacitance (C_{ox}) increases and the overdrive voltage $(V_{gs} - V_{th})$ is lower with technology scaling. The line resistance, however, is a strong function of technology, increasing with each technology generation. The ratio of the line resistance to the driver resistance (R_{line}/R_s) therefore increases with each technology generation.

The effect of R_{line}/R_s on the crosstalk noise voltage is shown in Fig. 10 for several interconnect line lengths (for the 65-nm technology node). As mentioned previously, with increasing driver resistance, physical spacing becomes more efficient than shield insertion since coupling from the shield line is greater than coupling from the aggressor. The shield line

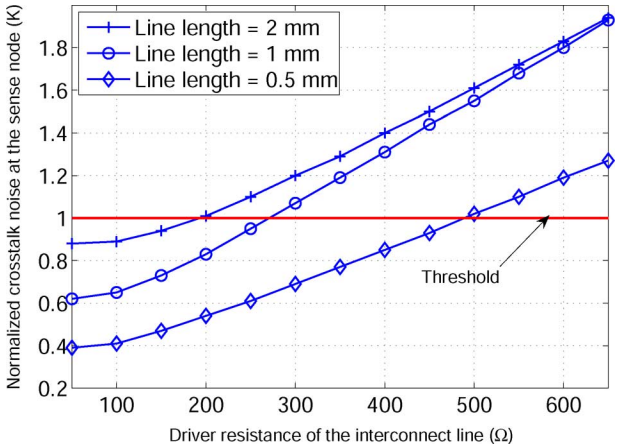

Fig. 10. Effect of $R_{\rm line}/R_s$ on the crosstalk noise voltage. The length of the interconnect line is 0.5, 1, and 2 mm.

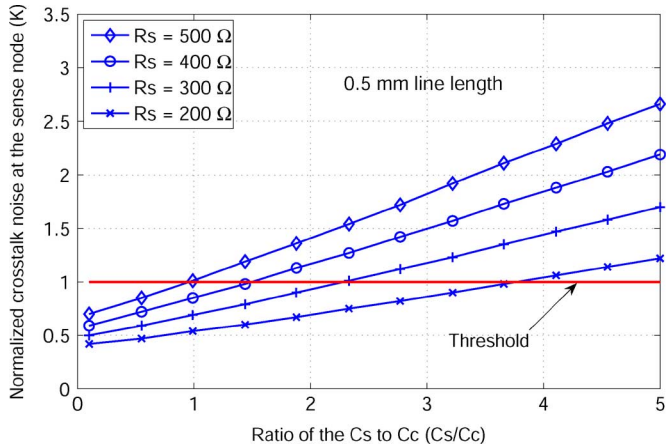

Fig. 11. Ratio of substrate capacitance to coupling capacitance versus normalized crosstalk noise when a P/G line is routed as a shield line. The interconnect length is 0.5 mm.

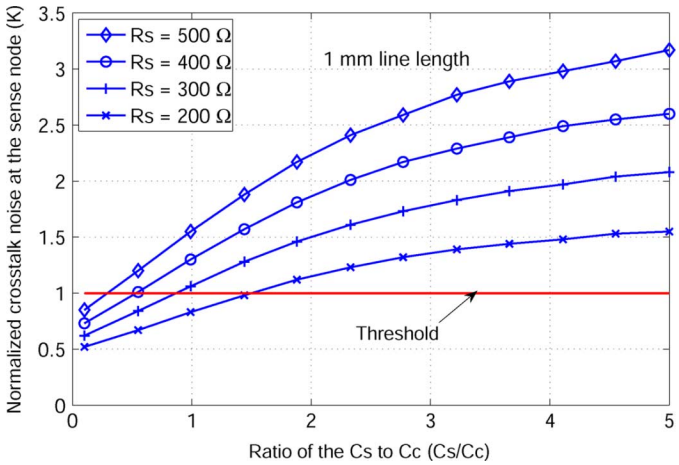

Fig. 12. Ratio of substrate capacitance to coupling capacitance versus normalized crosstalk noise when a P/G line is routed as a shield line. The interconnect length is 1 mm.

exhibits no driver resistance so the P/G noise propagates to the sense node through the shield line whereas the aggressor noise voltage is attenuated by the large driver resistance at the near end of the aggressor line. Alternatively, when the driver resistance is small, coupling from the aggressor dominates the P/G noise, making shield insertion preferable. Another observation is that the length of the interconnect significantly affects the speed, power, and area characteristics when choosing between spacing and shielding methodologies in a noisy environment. Spacing is preferable when the interconnect is longer whereas shielding is preferable for shorter interconnect lines, as shown in Fig. 10. Additionally, the $R_{\rm line}/R_s$ ratio increases in more advanced technologies. The crosstalk noise voltage is therefore more sensitive to P/G noise on the shield line. Either the driver resistance or the line width should be reduced in more advanced technologies.

E. Effect of the Ratio of Substrate Capacitance to Coupling Capacitance on Crosstalk Noise

The coupling capacitance between adjacent interconnect strongly depends upon the switching activity of the wires [32]. When the signals driving the adjacent lines switch in the same direction, the coupling capacitance is the same as the coupling capacitance between two adjacent quiet lines. When the signals driving the adjacent lines switch in the opposite direction, the coupling capacitance between the adjacent lines is two times the capacitance when only one of the adjacent lines is switching [32], [33].

The effect of the ratio of the line-to-substrate capacitance to the coupling capacitance has been evaluated for active and passive shielding structures [11], but without considering P/G noise on the shield lines. The effect of this ratio on the crosstalk noise at the sense node for different driver resistances is depicted in Figs. 11 and 12 for interconnect line lengths of 0.5 and 1 mm, respectively. When the coupling capacitance is greater than the line-to-substrate capacitance, shield insertion is more effective than additional spacing. As the line-to-substrate capacitance becomes greater than the coupling capacitance, physical spacing becomes more efficient than shield insertion. For example, when R_s is equal to 300 Ω, spacing is preferred when C_s/C_c is greater than 2.3 for a 0.5 mm long line whereas for a 1 mm long line, spacing is preferred when C_s/C_c is greater than 0.9. The C_s/C_c ratio decreases with technology scaling, making shield insertion more effective than spacing in reducing the crosstalk noise.

F. Effect of Self- and Mutual Inductance on Crosstalk Noise

The self- and mutual interconnect inductance strongly depend on the technology and design parameters, as tabulated in Table II. The effect of changes in the width, thickness, and spacing between the interconnects differs significantly for self- and mutual inductance. The self-inductance is constant for a range of mutual inductance between $0.5L_s$ to $1.2L_s$ for different driver resistances. When the ratio of L_m/L_s increases, spacing is more effective in reducing the crosstalk noise, as depicted in Fig. 13. The crosstalk noise voltage generated at the sense node increases for both physical spacing and shield insertion when the L_m/L_s ratio increases. The increase in crosstalk noise voltage with shield insertion is however relatively high as compared to the increase in the crosstalk noise voltage with physical spacing. The reason is that the noise coupled from the shield line is physically closer to the victim line than the noise coupled from the aggressor line. The relative effect of the change in the mutual inductance is therefore higher in shield insertion

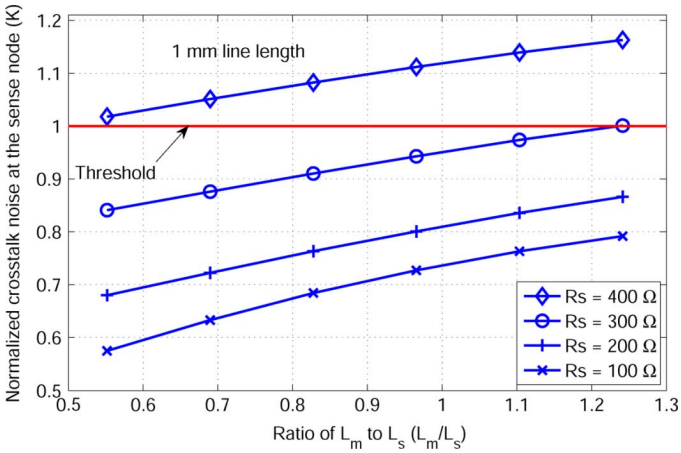

Fig. 13. Ratio of self-inductance to mutual inductance versus normalized crosstalk noise when a P/G line is routed as a shield line. The interconnect length is 1 mm.

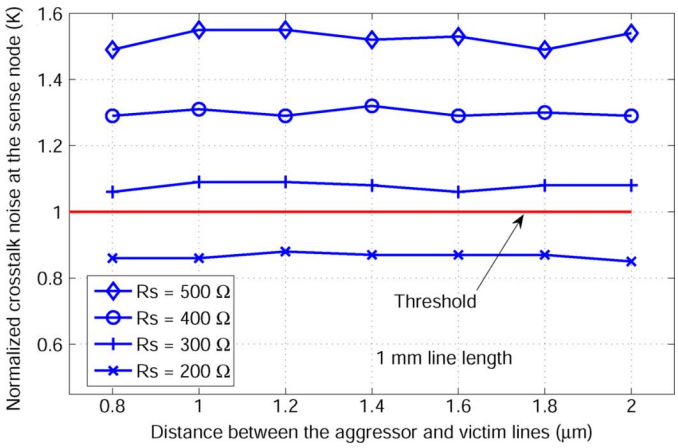

Fig. 14. Normalized crosstalk noise when a P/G line is routed as a shield line where the distance between the aggressor and victim line is varied from 0.8 to 2 μm. The interconnect length is 1 mm.

than physical spacing. This result is in good agreement with the results described in Section III-C.

G. Effect of Distance Between Aggressor and Victim Lines on Crosstalk Noise

The crosstalk noise at the sense node is inversely proportional to the distance between the aggressor and victim lines since the coupling capacitance and mutual inductance decreases with increasing separation between lines. In this section, the effectiveness of shield insertion in a noisy environment is discussed. L_m decreases with greater separation between adjacent wires, lowering the L_m/L_s ratio. Alternatively, the C_s/C_c ratio increases with higher separation. Shield insertion is more efficient with a smaller L_m/L_s ratio. Conversely, additional spacing is preferable with a higher C_s/C_c ratio. The ratio $V_{\text{sense\_with\_shielding}}/V_{\text{sense\_with\_spacing}}$, denoted as K, therefore does not change significantly with increasing separation between the aggressor and victim lines. The distance between the aggressor and victim lines is varied from 0.8 to 2 μm, where the ratio of the crosstalk noise generated at the sense node with both shield insertion and spacing is shown in Fig. 14. Note that when comparing the effectiveness of shield insertion to physical spacing, the separation between the aggressor and victim lines is the same for both techniques.

IV. Summary: Shield Insertion or Physical Spacing in a Noisy Environment

The decision criterion to choose between shield insertion and physical spacing in a noisy environment is summarized in this section. Shield insertion and physical spacing between adjacent interconnect are evaluated for several interconnect lengths and shield widths. Shield insertion is shown to be more efficient for shorter and narrower lines while additional space is preferable for longer and thicker lines. The effect of the driver resistance of the victim and aggressor lines on the crosstalk noise has also been investigated. Shielding is preferable for smaller driver resistance and physical spacing is preferable for higher driver resistance. The ratio of the substrate capacitance to the coupling capacitance is explored in terms of mitigating coupling noise. Shield insertion is preferable for those lines with higher coupling capacitance than the line-to-substrate capacitance. Furthermore, when the mutual inductance between adjacent lines becomes higher than the self-inductance of the line, physical spacing becomes more efficient as compared to shield insertion in a noisy environment. A summary of the decision criteria is listed in Table IV for different technology nodes.

TABLE IV
Decision Criterion for the Critical Interconnect Length (Width), $R_s = 300\ \Omega$. Shield Insertion is Preferable When the Interconnect Length (Width) is Smaller Than the Critical Length (Width). Spacing is Preferable When the Interconnect Length (Width) is Greater Than the Critical Length (Width)

	Technology node	Shielding	Critical dimension	Spacing
Length[a]	65 nm	✓ <	1 mm	< ✓
	45 nm	✓ <	0.9 mm	< ✓
	32 nm	✓ <	0.2 mm	< ✓
Width[b]	65 nm	✓ <	0.7 μm	< ✓
	45 nm	✓ <	0.9 μm	< ✓
	32 nm	✓ <	1.2 μm	< ✓

[a]Width is maintained at 1 μm
[b]Length is maintained at 1 mm

A practical design example is analyzed that exemplifies the importance of P/G noise on the shield line when choosing between shield insertion and spacing. The circuit is shown in Fig. 3. Four different scenarios is considered: 1) a noise-free shield line; 2) a shield line with 40 mV peak noise; 3) a shield line with 100 mV peak noise; and 4) no shield line (physical spacing). The distance between the aggressor and victim lines is the same for shield insertion and physical spacing. The results are illustrated in Figs. 15 and 16 for 0.5 and 1 mm interconnect lengths, respectively. For both cases, the crosstalk noise is greatest with a shield line with 100 mV P/G noise. The decision criteria, however, change when the P/G noise is 40 mV. For a 0.5 mm line length, the maximum noise with a shield line is greater than the noise without a shield line. The maximum noise with a 1 mm line is however greater without a shield line as compared to a shield line with 40 mV P/G noise. Additionally, when no P/G noise is present on the shield line, shield insertion is the preferred design method to mitigate crosstalk noise.

Two of the most important parameters to consider when choosing between shield insertion and physical spacing is the

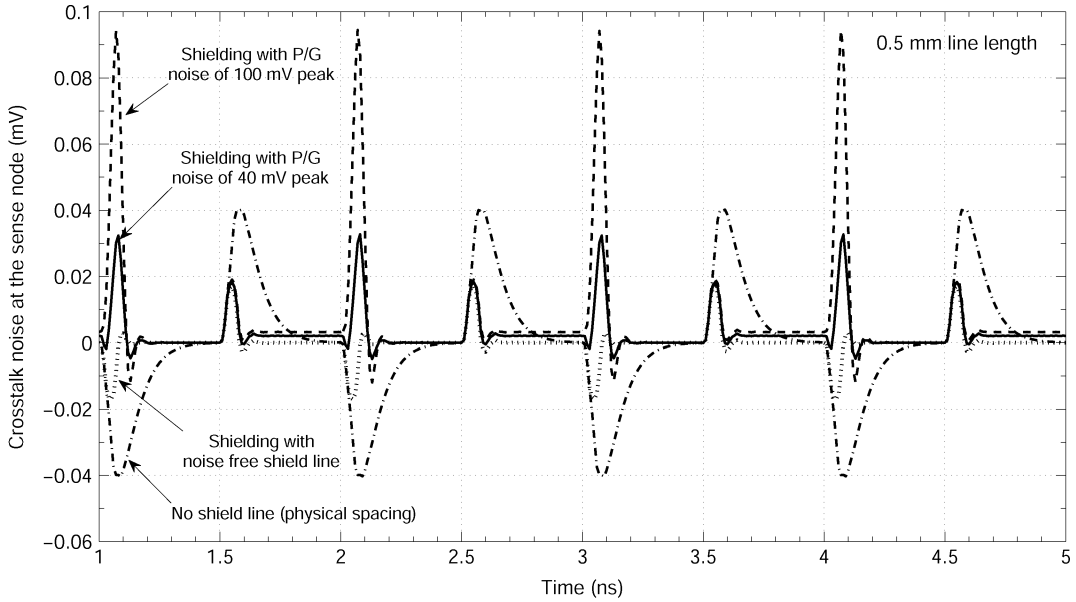

Fig. 15. Crosstalk noise at the sense node with an inserted shield line with different noise profiles (noise free, 40, and 100 mV P/G noise on the shield line) and without a shield line (physical spacing). The interconnect length is 0.5 mm.

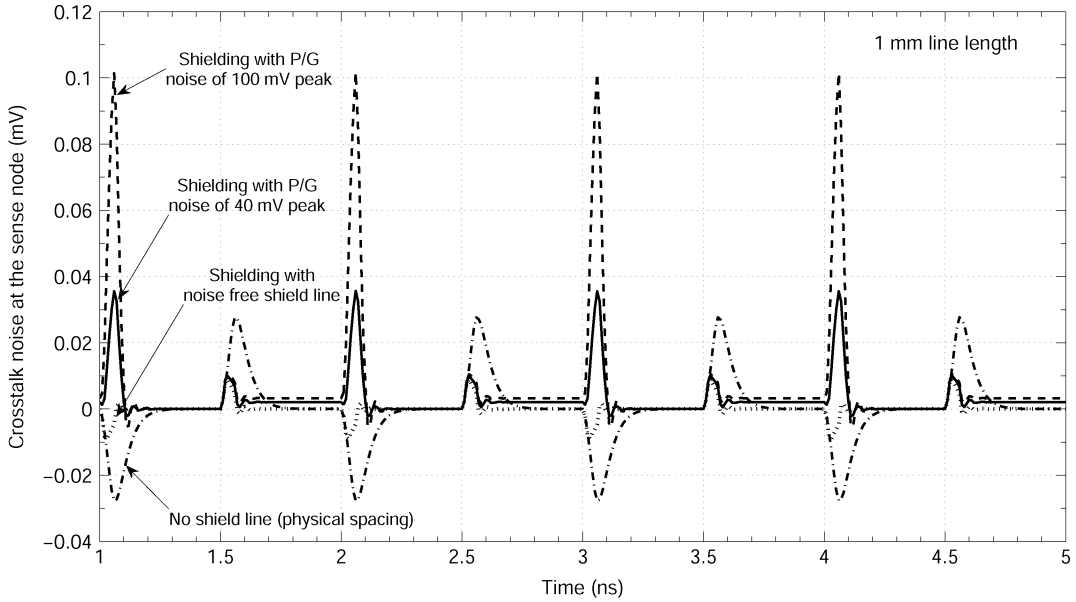

Fig. 16. Crosstalk noise at the sense node with an inserted shield line with different noise profiles (noise free, 40, and 100 mV P/G noise on the shield line) and without a shield line (physical spacing). The interconnect length is 1 mm.

interconnect line length and the size of the transistors driving the aggressor and victim lines. For short interconnect lines, shield insertion is preferable while physical spacing is preferred for longer lines. This decision, however, also strongly depends upon the output resistance of the driver transistors and the width of the interconnect lines, as explained in Section III. When R_s becomes smaller (i.e., a stronger driver strength), shield insertion is more efficient in reducing crosstalk noise.

V. Conclusion

Shielding methodologies in the presence of P/G noise are introduced in this paper. With technology scaling, P/G noise has become a significant design issue. The P/G network has become more resistive, increasing the noise within the P/G distribution network. Additionally, with supply voltage scaling, the noise of the P/G network is more significant. P/G noise is the dominant source of crosstalk noise when the noise is greater than 7% of the supply voltage. Coupling from the aggressor to the victim is the dominant noise source when the P/G noise is less than 2% of the supply voltage. The P/G noise on the shield line reduces the efficiency of shielding because this noise also couples to the victim lines. The effect of technology scaling on shield insertion in a noisy environment has also been investigated.

Appendix
Closed Form Expressions For Interconnect Resistance, Capacitance, and Inductance

Closed-form expressions for the resistance, capacitance, and inductance of a line are summarized in this section to provide additional background on the effect of technology and certain

design parameters on the interconnect impedance. The interconnect line resistance is

$$R = \frac{\rho L}{WT} \tag{2}$$

where ρ, L, W, and T are the resistivity, length, width, and thickness of the interconnect, respectively. The line-to-substrate capacitance and coupling capacitance, respectively, are [34]

$$\begin{aligned}\frac{C_s}{\varepsilon_{\text{ox}}} &= \frac{W}{h} + 2.2217\left(\frac{s}{s+0.7h}\right)^{3.193} \\ &\quad + 1.171\left(\frac{s}{s+1.51h}\right)^{0.7642} \\ &\quad \times \left(\frac{T}{T+4.532h}\right)^{0.1204},\end{aligned} \tag{3}$$

and

$$\begin{aligned}\frac{C_c}{\varepsilon_{\text{ox}}} &= 1.144\frac{T}{s}\left(\frac{h}{h+2.059s}\right)^{0.0944} \\ &\quad + 0.7428\left(\frac{W}{W+1.592s}\right)^{1.144} \\ &\quad + 1.158\left(\frac{W}{W+1.874s}\right)^{0.1612} \\ &\quad \times \left(\frac{h}{h+0.9801s}\right)^{1.179}\end{aligned} \tag{4}$$

where ε_{ox}, h, and s are the oxide permittivity, distance from the interconnect to the substrate, and spacing between adjacent interconnects, respectively. Closed form expressions for the self- and mutual inductance of a line, respectively, are [35], [36]

$$L_s = \frac{\mu_0 \cdot L}{2\pi}\left[\ln\left(\frac{2L}{W+T}\right) + \frac{1}{2} + \frac{0.22(W+T)}{L}\right] \tag{5}$$

and

$$L_m = \frac{\mu_0 \cdot L}{2\pi}\left[\ln\left(\frac{2L}{d}\right) - 1 + \frac{d}{L}\right] \tag{6}$$

where μ_0 and d are, respectively, the magnetic permeability of free space and the center-to-center distance between two adjacent interconnects.

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